VERY LARGE TELESCOPE

TECHNICAL SPECIFICATION
MACAO
APD Counter Module

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1. Introduction

When light passes through the atmosphere, it is often distorted due to inhomogeneous air temperature and other effects. This distortion is undesirable for astronomical observations. It is, however, possible to compensate for this in real-time with a system that analyzes the distortion and improves the image by acting on a deformable mirror in the optical path. Such a system is referred to as an Adaptive Optics System.

A central element in this Adaptive Optics System is an APD Counter Module. (ACM). It acts as an interface between an array of 60 Avalanche Photo Diodes (APD) and a Real Time Computer (RTC). Figure 1.1 shows a system block diagram.

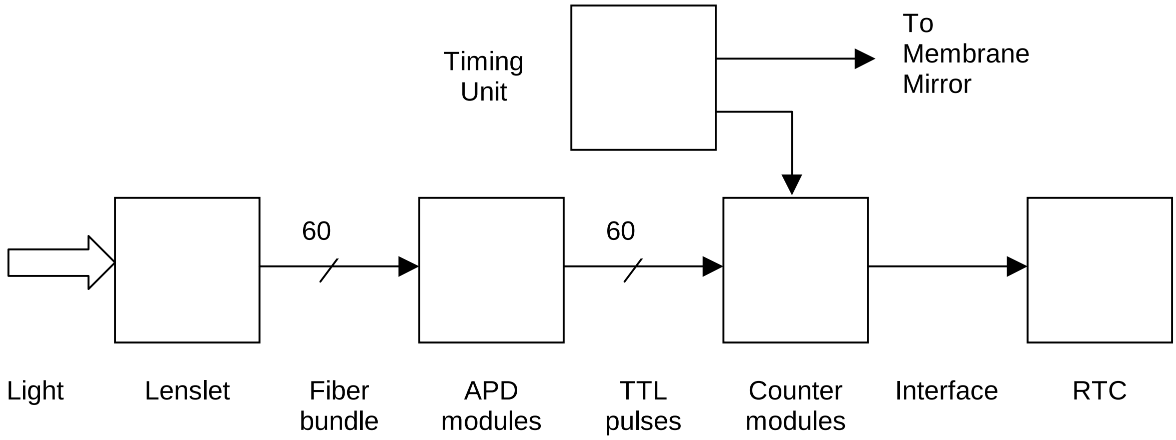

Figure 1.1 Simplified System Block Diagram

1.1. Purpose

ESO will need to acquire APD counter modules required for the ESO in-house developed AO system MACAO. This document lists technical requirements for the APD counter modules, and also presents a delivery schedule.

1.2. Scope

Electronics requirements are outlined in Chapter 2, and Chapter 3 contains interface requirements. In Chapter 4 mechanical requirements are found. Deliverable documentation is listed in Chapter 5 and delivery schedule in Chapter 6.

1.3. Applicable Documents

None.

1.4. Reference Documents

None.

2. Electronics Requirements

2.1. Counter Module Requirements

The APD counter module shall consist of 2 banks of 60 counters, each 16 bit wide. The counting is controlled by a remotely programmable timing unit that generates a sine wave signal with a remotely programmable amplitude, phase and frequency in the range of 1.5 to 3 kHz. The sine wave is used to drive the membrane mirror which periodically defocusses the image on the APD array. The membrane mirror is driven by a voice coil similar to a dynamic loudspeaker. The timing unit also generates control signals which are freely configurable in phase with respect to the sine wave. These control signals enable the counting of the first counter bank during the first half cycle and counting of the second bank during the second half cycle. Furthermore signals to transfer the counter values to a FIFO or Dual Port RAM are required. The such generated 16-bit values are transferred over a parallel interface or fibre link to the RTC which performs the numerical computations for the AO control loop. A simplified timing diagram is shown below.

The configuration of the timing parameters shall be freely programmable via registers accessible by the RTC over the fibre link or VME interface.

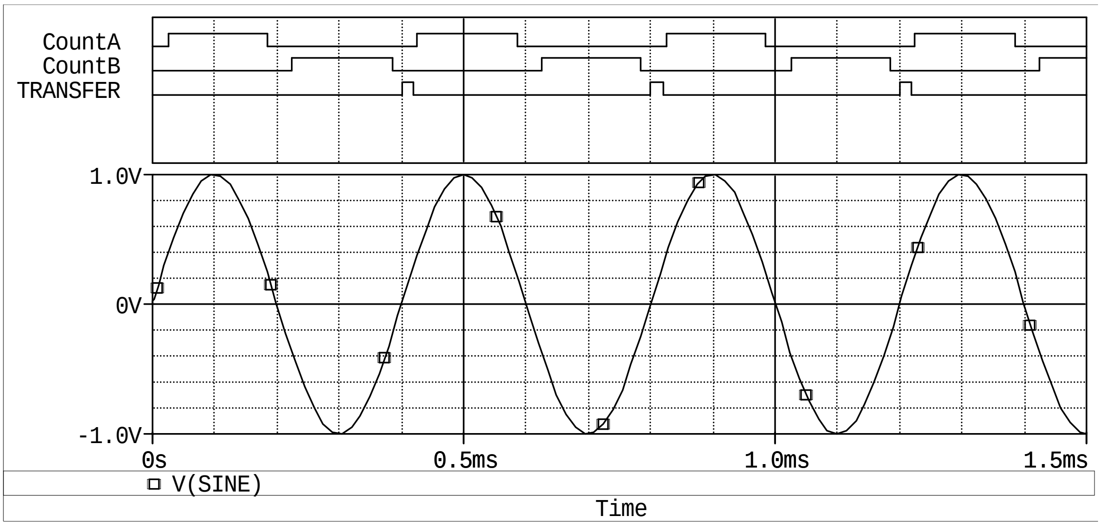

Figure 2.1 Simplified Timing Diagram

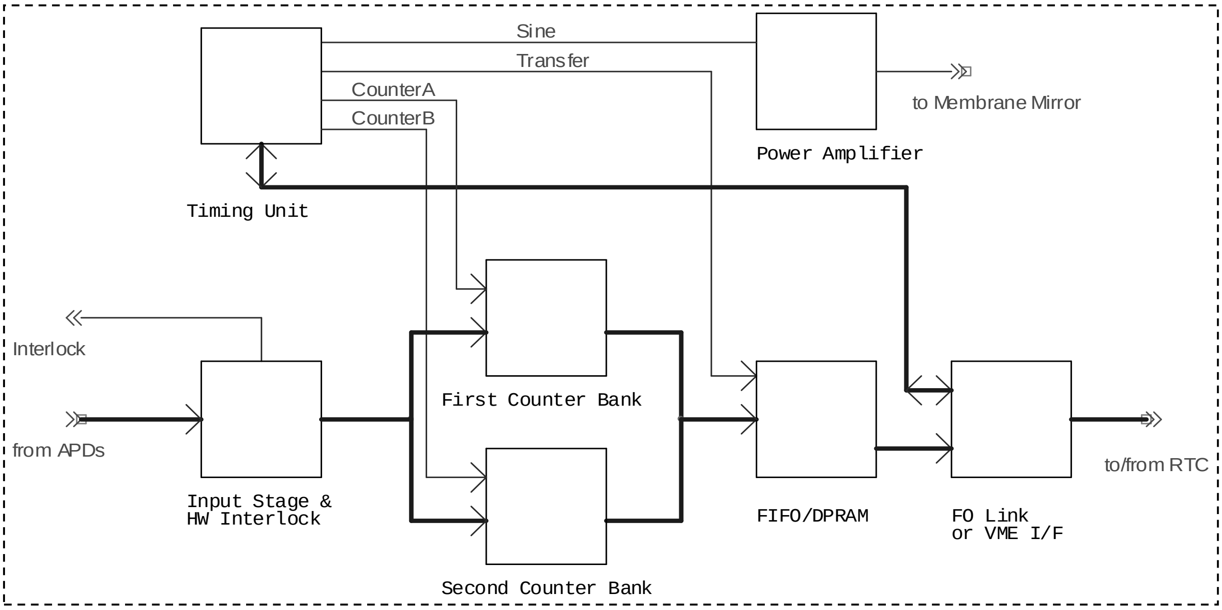

Figure 2.2 Simplified ACM Block Diagram

The Real Time Computer calculates corrective signals for the deformable mirror output voltage values. Values are passed to the instrument LCU (Local Control Unit) and from there to the HV driver.

Interlocks are required in order to protect the APD modules from excessive light.

A hardware interlock shall be incorporated into the ACM. It shall monitor the count rate of the APDs and generate a control signal that enables the APD power supply as long as the count rate is below a threshold of 2MHz. The interlock signal shall be latched and remotely controlable via the interface to the RTC. The signal must be active to turn APD power on. The signal shall be set to the non-active state during power-on reset of the ACM. A front panel LED shall indicate the state of the interlock signal. It should be possible to disable all status LEDs to avoid light pollution.

In addition to the hardware interlock the RTC will monitor the APD count rate. If this value will exceed a certain limit, the RTC SW will take the following actions:

- Close protective shutter
- Move ND wheel to its blocking position
- Remove power to APDs

2.1.1. Hardware Deliverables

A simplified block diagram of the APD counter module can be found in Figure 2.2. Parts inside the dashed line are deliverables, and considered as part of the counter modules system. These are:

- High-speed interface to RTC (either fibre link or VME bus I/F)
- Input interface for APD signals
- Input/Output interface to VME/RTC
- Output interface to membrane mirror (i.e. a car audio power amplifier)
- Output interface for APD power interlock

2.1.2. ESO defined and supplied Parts

The following parts are outside the scope of work, and will be supplied by ESO:

- Real time computer Motorola PPC Model 2604.
- APD modules
- APD power supply

2.2. Counter Module Specification

- Minimum number of counters 2x60
- Single-ended (TTL) or differential (RS-422) input
- Minimum count rate from DC to 15 MHz
- Frequency range of sine wave generator 1.5…3kHz
- Resolution of sine wave amplitude >=12 bits
- Resolution of sine wave frequency <= 1Hz
- Power amplifier bandwidth (-3dB) 500Hz…9kHz
- Maximum output power >=4W into 4 Ohms
- Distortion of power amplifier <= 5% at max. power
- High speed fibre link or VMEbus I/F
- Dual ported RAM or FIFO for data buffering
- Interlock output for APD power supply

2.3. Power Consumption

The power consumption should be kept as low as possible.

2.4. Service and Maintenance

Measuring points shall be provided at the APD signal inputs, the sine wave D/A output and timing unit signals.

2.5. EMC

As this unit will operate with high frequency signals close to sensitive CCD readout electronics, it is extremely important to minimize any EM radiation. Shielding and proper grounding schemes are essential.

2.6. Plug'n'Play

It must be possible to replace any board without re-calibration or board configuration (exception: board address coding).

2.7. Power Supply

Conforming to VMEbus specification in the case of a VMEbus based system, 230VAC in case of a standalone system.

2.8. Altitude

The counter module must be capable of operating at an altitude of 2.800 metres above sea level (Paranal observatory).

3. Interface Requirements

3.1. Interface to Real Time Computer

The interface to the real time computer (RTC) should either be a standard A32D32 VMEbus interface or a high speed fibre link. In case of a fibre link is chosen the preferred solution for the host end of the fiber link the will be a PMC card mountable in the RTC, which is a Motorola PPC Model 2604 running VxWorks 5.3.

One example of a board implementing a PMC to fiber link using the Cypress HOTLink chipset is the FPMC-HL266 from TEK Microsystems

http://www.tekmicro.com/products.fastlinks.fpmc-hl266.html.

- Transfer Rate: >= 20 Mbyte/s
- Latency: Time from end of counting half period to last data word sent to RTC <100us
- Distance: The fiber link should be capable of being at least 300m in length

3.1.1. Data Format

16-bit words x 120. In the case of a VMEbus board with FIFO or DPRAM an interrupt shall be generated on valid data. In the case of a fibre interface the data shall be sent as a vector with an appropriate sync mechanism.

3.1.2. General

Fiber link must not be emitting (leaking) light at any wavelength.

3.2. Selftest

A simple selftest functionality like reading back configuration register contents shall be provided.

3.3. Interface to Interlock

The interlock signal must be able to drive a relay of type Siemens V23042-DPDT or equivalent.

3.4. Connectors

3.4.1. Fiber Connectors

For fiber interface connectors, refer to Section 3.1.

3.4.2. APD Connectors

TBD

3.4.3. Interlock Connector

TBD

4. Mechanical Requirements

4.1. Form Factor

The board(s) shall comply with the double euro board form factor.

4.2. Unit Identification Label

Each unit shall be clearly labeled for identification purposes. At least the following information shall be included:

- Unit name
- Unit serial number
- Manufacturer
- Manufacturing date
- Power supply voltage, frequency and current

5. Documentation

The following documentation shall be delivered with each APD counter module:

1. Users manual
2. Installation manual
3. Maintenance and troubleshooting manual
4. Acceptance test protocol

To be delivered with the first system:

5. Schematics for all boards
6. Backplane protocol description (if applicable)

All documentation shall be in English. If possible, in addition to paper documentation, electronic documentation is considered valuable. All documentation must be delivered before, or together with the delivery of the first system.

6. Project Schedule

6.1. Project Phase Definition

The following milestones (**in bold**) and project phases (*italic*) are identified:

T0	**Kick-off meeting**
Phase 1	*Design phase*
T0 + 3 months	**Design report submitted to ESO for review**
Phase 2	*Manufacturing phase*
T0 + 5 months	**Delivery and acceptance test of Unit #1 and documentation according to Section 5 of this document**
Phase 3	*Series manufacturing of unit #2-#7*

6.2. Delivery Schedule

A total of 7 fully tested units are required. The first unit shall be delivered at the latest five months after contract award. Following delivery and acceptance of the first unit, ESO will require one unit every three months. Earlier delivery than proposed, or delivery of more than one unit at once, is accepted and encouraged. The above delivery scheme is to be considered as maximum delivery times.

The supplier shall propose a development and production planning which will meet the above schedule. This information is to be considered as a part of the bid, and must be presented clearly and separately.

7. Acceptance Procedure

Each unit shall be going through an acceptance test upon delivery to ESO, and a test report shall be written for each unit. The test shall be performed by the supplier, in co-operation with ESO. The test procedure shall be produced by the supplier, and submitted to ESO for approval before delivery of the first unit

The following tests shall be performed for each unit:

1. Performance according to section 2 of this document
2. High speed link or interface functionality
3. Selftest functionality as specified in section 3.2 of this document

The following tests shall be performed for the first unit only:

4. Power consumption at idle condition
5. Conducted EMC test (performed by ESO specialist using ESO test equipment)
6. Electrical safety check (performed by ESO specialist using ESO test equipment)
7. Review of documentation according to section 5 of this documentation

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