MACAO
APD COUNTER MODULE
DESIGN REPORT

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Contents

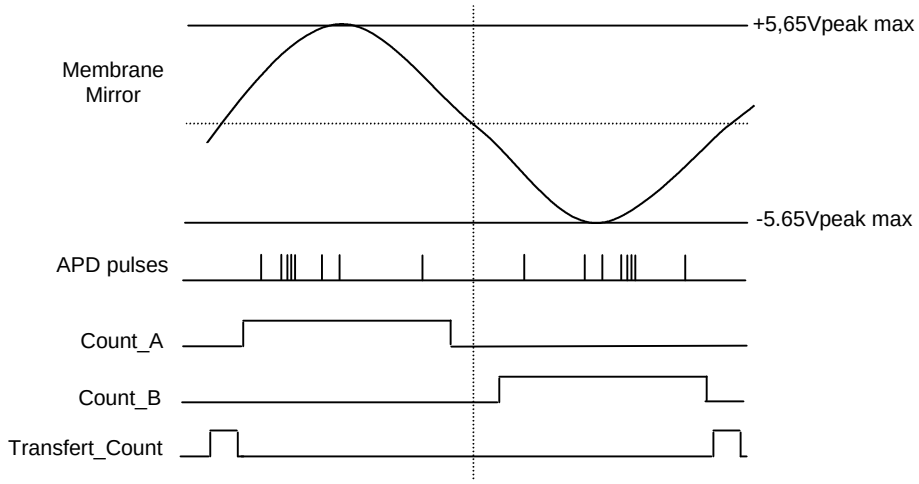
1. SCOPE

This document is the Design Report of the APD Counter Module for the MACAO instrument.
This issue is written for the FDR of 14 March 2001.

The APD Counter Module is a VME Slave Board with dedicated hardware to collect 60 differential APD signals and to count their pulses synchronised with a square wave.
The board supplies the interlock signal which controls the power of APD.

In parallel, the board generates a sinusoid controlled in amplitude, in frequency and in phase (with square wave).

Principle scheme :



The user needs :

- to define the frequency and the amplitude of the sinusoid,
- to define the square wave associated to counter A and the square wave associated to counter B,
- to define the shift between sinusoid and “square wave counter A + square wave counter B”,
- to configure the interlock system .

The user needs to have the capability to tune the sinusoid frequency and to adapt the sinusoid amplitude without opening the Adaptive Optics loop.

2. ACRONYMS AND ABBREVIATIONS

EMC	Electro Magnetic Compatibility.
EMI	Electro Magnetic Interference.
MACAO	Multiple Application Curvature Adaptive Optics.
ACM	APD Counter Module.
FPGA	Field Programmable Gate Arrays.
VHDL	Very High Description Language.

3. APPLICABLE AND REFERENCE DOCUMENTS

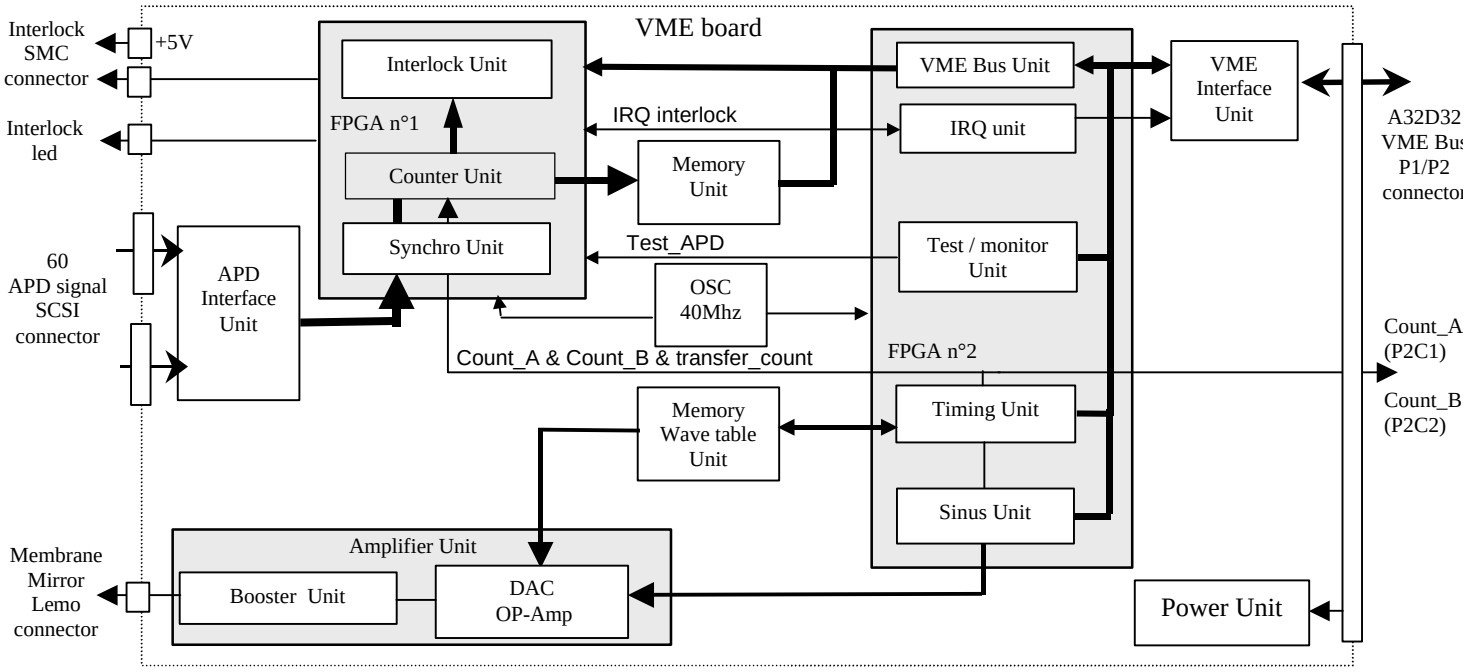
Technical Specification MACAO APD Counter Module, Doc No VLT-SPE-ESO-11640-2262 Issue 1.0 date 03/08/00.

Proposal MACAO APD Counter Module, Doc No SHK-RTE-PRJ-00010 Issue 1.0 date 29/09/00.

Addendum on the Proposal MACAO APD Counter Module, Doc No SHK-RTE-PRJ-00010 Issue 1.1 date 24/11/00.

4. ACM ARCHITECTURE DETAILLED DESCRIPTION

4.1. Logical cutting out diagram



4.2. APD interface unit

4.2.1. Hardware characteristics

Type of unit : Numeric (TTL).

Main components :

- 2 SCSI connectors 68 cts shielded receptacle right angle. Ref: AMP 787171-7
- 15 Quad differential line receiver. Ref NS DS26C32ATM.

Power : +5Volts.

Consumption : 350 mA max.

Schematic : Eg. Annexe n° 1 p47 to p51.

4.2.2. Features

We use two SCSI connectors in front face panel to recover the 60 differential APD signals.
The APD signals are transferred in TTL format with a RS422 receiver.

4.2.3. Note

Beware at the ESO request, we supply the power (+5v) on the SCSI connector.
This power is filtered (EMI filter) and we implant a fuse with the board power.

ESO must check the use of this power, in particular the consumption and the ground reference.
Beware the EMC interference on the power line.

This consumption is not integrated in total consumption.

4.3. FPGA N°1

This FPGA is dedicated to APD counters.
The goal is to synchronize the APD signals with our basic clock, to count their pulse in reference to square enable signals.
It oversees the counter value and supplies the interlock signal.
It memorizes the counter value in a Dpram module (memories unit).

4.3.1. Hardware characteristics

Type of unit : Numeric (TTL).

Main components :
- FPGA. Ref: Xilinx XC4036XLA-09HQ240I.
- Prom configuration. Ref: Xilinx XC1701LPC20I .

Power : 500mA peak (during configuration), about 300mA in working.

Consumption : +3.3Volts.

Schematic : Eg. Annexe n° 1 p52 & p53

FPGA characteristics :
- Max frequency post layout : 50 Mhz.
- Occupation rate : 85% (25 Kgates equivalent).
- Pinout number : 120/193.

4.3.2. Synchro Unit

Because the APD signal waveform specification is very hard (pulse width min 25 ns with a dead time min 40ns) we synchronise all APD signals on our basic clock (40MHz), an installation with RS flip flop plus an anti-metastability system is implanted in the design.

At each pulse rising edge, we increase a dedicated counter.

4.3.3. Counter Unit

The Counter unit is composed of 1 banks of 60 counters each 12 bits.

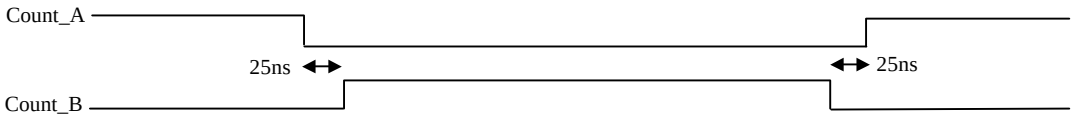
The counting is enabled by two square enable signals coming from Timing Unit (namely Count_A and Count_B). We count if one of these 2 signals is enable.

The transfer in the memory bank is made in two steps:
- 60 counters at the end of Count_A signal.
- 60 counters at the end of Count_B signal.

Remarks on the bit width:
The counting rate is limited to an average frequency of 2 Mhz, the maximal coding value is acquired with the slower frequency of the square signal.
2Mhz / 1.5 Khz gives less than 1340 counts and our bit width is 12 bits (4095 counts).

4.3.3.1. NOTE

In order to have a good transfert after each square wave signal (Count_A and Count_B), we need a dead time of 1 clock cycle (25ns).



4.3.4. Interlock Unit

4.3.4.1. HARDWARE CHARACTERISTICS

Type of unit : Numeric (TTL)

Main components :

- 2 NPN transistors. Ref: fairchild MMBTA42.
- 2 SMC connectors. Ref: radiall R112665.
- Led. Ref: agilent HLMP-NG07.

Power : +5Volts.

Consumption : 50mA (if interlock active).

Schematic : Eg. Annexe n° 1 p52.

4.3.4.2. FEATURES

This unit monitors the count rate of all APDs.
It supplies the interlock signal and interlock led on the front face panel.
It drives an IRQ on the VME Bus.

If one counter exceeds a value written by software (via interlock count data register), the interlock signal is active. This check is performed automatically each time at the end of counting.
The interlock signal is latched and remotely controlable (via interlock system register).

The interlock signal is combined with a pull-down resistor and NPN transistor to drive a relay .
The signal ouput is in open collector during power on reset.

Note : we have implanted a free wheeling diode on the board for the relay but we recommend that the relay has also a free wheeling diode.
In fact, if there is not a free wheeling diode integrated, the cable conducts the overvoltage up to our board (beware for the EMC requirements).

On the front face panel, we have one SMC connector for the interlock signal and one SMC connector for the power of interlock relay.

Between the power interlock relay connector and the +5V supply, we have put a fuse and an EMI filter.

A front panel LED indicates the state of the interlock signal, it is possible to disable (via interlock system register).

An IRQ (BusVME) is supplied when the interlock signal is active, we keep the possibility to mask this IRQ (via the IT system register).

In every case (IRQ enable or disable), if the interlock system detect a saturation we shutdown the APD power through interlock signal AND we signal it in IT system register.

4.4. Memory Unit

4.4.1. Hardware characteristics

Type of unit : Numeric (TTL).

Main components : 2 Dual port static RAM. Ref: cypress CY7C133-25JI.

Power : +5Volts.

Consumption : 340mA.

Schematic : Eg. Annexe n° 1 p52.

4.4.2. Features

A 32 bits DPRAM is implemented as an interface between the ACM and the CPU board.

The data transfert is possible in VME32BLT mode.

The maximum rate transfert depends on the VME Master board.
The theorical pure delay between the first and the last data read is 4,8µs in BLT mode.

The memory is described as below:

Address	Data_MSB (31-16)	Data_LSB (15-00)
0	CountA_APDin1	CountA_APDin0
…	…	…
29	CountA_APDin59	CountA_APDin58
30	CountB_APDin1	CountB_APDin0
…	…	…
59	CountB_APDin59	CountB_APDin58
60	CountB_APDpulse_test	CountA_APDpulse_test
61	A5A5	Count_trame

The trame_indice corresponds at :
- 0 if square wave CountA ,
- 1 if square wave CountB.

The Count_trame is the value of the trame (15 bits), this value is remotely controlable (via interlock register system).

4.5. VME interface Unit

4.5.1. Hardware characteristics

Type of unit : Numeric (TTL).

Main components :
- 2 20 bits Bus interface D-type latches tristate. Ref: TI SN74ABT16841DL.
- 2 16 bits Bus transceivers tristate. Ref: fairchild 74ABT16245CSSC.
- 2 quad NAND buffer (Open collector). Ref: fairchild 74F38SC.
- 1 octal bidirectional transceivers tristate. Ref: fairchild 74ACT245SC.
- 2 connectors DIN41612. ref: harting 09-03-196-6921.

Power : +5Volts.

Consumption : depends on VME bus activities 700mA peak. 300mA average.

Schematic : Eg. Annexe n° 1 p58.

4.5.2. Features

This unit answers at the VME Bus electrical interfaces.

4.6. FPGA n°2

This FPGA is dedicated to VME bus interface and generated the sinusoid and square wave signals.
It supplies also an APD test pulse to answer to self test, monitoring and maintenance requirements.

4.6.1. Hardware characteristics

Type of unit : numeric (TTL).

Main components :
- FPGA. Ref: Xilinx XC4036XLA-09HQ240I.
- Prom configuration. Ref: Xilinx XC1701LPC20I.
- Rotary dip switches. Ref: apem PT65103.

Power : 500mA peak (during configuration), about 300mA in working.

Consumption : +3.3Volts.

Schematic : Eg. Annexe n° 1 p56 & p57.

FPGA characteristics :
- Max frequency post layout : 48 Mhz.
- Occupation rate : 42% (12.5 Kgates equivalent).
- Pinout number : 191/193.

4.6.2. VME Bus Unit

This unit generates the signals to control the VME Bus interface unit in Slave.
It contains the state machines to answer to different access :
- Read/write normal mode on 16 bits,
- Read BLT mode on 32 bits,
- IRQ.

This unit compares the physical address board to VME address Bus to check an access.
The physical address board is configurable via 3 rotary dip switches (hexadecimal) which represent the MSB (31-20) VME Bus address.

The board has an 20 bits address space.

4.6.3. IRQ Unit

This unit contains the IT system register to affect the different interrupts (Interlock, Transfer count) to an IRQ VME level.
This register has an option to mask the IRQ.

4.6.4. Test and monitor Unit

To answer to self test, monitoring and maintenance requirements, we deliver a calibrated signal, where the width and the dead time are programmable by tick of 25ns (via APD test pulse data and system registers).
This unit checks the right functionning of FPGA n° 1 (synchro unit, counter unit, timing unit, memory unit, interlock unit).

4.6.5. Timing Unit

This unit controls the wave table memory bank supplies two square wave signals (Count_a and Count_B) and one pulse signal (Transfert_Count) to the counter unit.

It drives an IRQ on the VME Bus.

This unit is combined with the sinus unit and amplifier unit to generate the sinus wave signal which drives the membrane mirror.

Our system is based on two banks of 32K*16 bits.

The data word is composed of :

	Bit 15	Bit14	Bit 13-12	Bit 11-0
Data	Count_B	Count_A	Blank	Data sinus wave

We can swap between the banks (via sinus system register) to adjust the sinusoid without opening the system loop.

The transfer of the allocation table is set to about 32ms.
To initiate the system, this operation has to be done at initialization.
When one bank is used to generate the sinusoid, we can write in parallel the other bank (via sinus system register).

Moreover, this system presents the advantage to have the control signals integrated with sinus generation and enables all possible phases and periods.
Two deviation phase registers are implemented (Count_A data and Count_B data register) to calibrate the square wave signal in relation with the sinusoid.
These registers are taken into account via Count system register.

At the end of each square wave signal, a pulse signal (Transfer_Count) is generated to transfer the counter value in the Dpram module (eg counter unit).

At the end of Count_B, an IRQ (BusVME) is supplied.

In order to respect the full 1Hz resolution , we have a sampling rate of 25ns.
(1Hz on 3Khz frequency gives a delay <110ns).

Our system has always the same sampling rate (40Mhz) depending on frequency (1.5Khz up to 3Khz), that implies we have a dynamic allocation table.
For 3Khz we have 13Ksample and for 1.5Khz we have 26Ksample.
This dynamic is software controllable via Table1_count data register and table2_count data register.

4.6.5.1. NOTE

At the ESO demand, we have output:

- Count_A signal on the P2-C1 connector,
- Count_B signal on the P2-C2 connector.

4.6.6. Sinus Unit

This units generates the signals to control the sinusoid chain in relation with amplifier unit.

We have one serial link for the amplitude reference DAC (16 bits).
With this component, we cover the sinusoid amplitude range of 0.565Vpeak to 5.65Vpeak.
This DAC is controllable via amplitude data register and amplitude system register.

We have one serial link for the attenuator component (8 bits).
With this component, we attenuate the sinusoid amplitude by step 0dB to -62 dB
This attenuator is controllable via attenuator data register and attenuator system register.

Moreover, we have the possibility to put in stand-by the sinusoid via the sinus system register.

4.7. Memory Wave Table Unit

4.7.1. Hardware characteristics

Type of unit : Numeric (TTL).

Main components :

- 2 Static RAM. Ref: IDT71016S15I.
- 2 16 bits buffer/drivers tristate. Ref: TI SN74ABT162244DL.

Power : +5Volts.

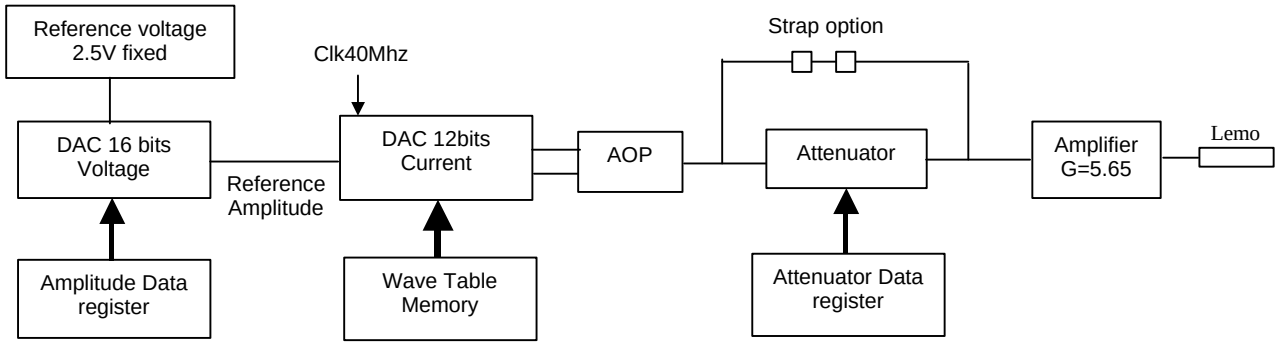
Consumption : 350mA.

Schematic : Eg. Annexe n° 1 p56.

4.7.2. Features

This unit contains two sinus wave tables.
These memories are read at 40Mhz, to improve the EMC requirement, we have chosen the data buffer component with serial resistors integrated.

4.8. Amplifier Unit



4.8.1. DAC and OP-Amp

4.8.1.1. HARDWARE CHARACTERISTICS

Type of unit : Numeric and analogic.

Main components :

- Low dropout voltage reference 2.5V. Ref: AD REF192GS.
- Voltage output 16 bits DAC. Ref: AD AD5541CR.
- 12Bits 125MPS TxDAC. Ref: AD AD9752AR.
- Voltage feedback amplifiers. Ref: AD AD8055AR.
- Audio Attenuator. Ref: NS LM1971M.
- High Speed amplifier. Ref: AD AD8051AR.

Power :+3.3V, +5V, +5VA, -5VA.

Consumption : +3.3V : 5 mA.
+5V : 2 mA.
+5VA : 80 mA.
-5VA : 35 mA.

Schematic : Eg. Annexe n° 1 p54 & p55 .

4.8.1.2.FEATURES

The reference voltage component gives a 2.5 Volts with a precision of 0.4%.

The DAC Voltage 16 Bits divides this reference (via sinus unit) to give a 0.1Vpk to 1Vpk of amplitude voltage range for the sinusoid with a total precision of +/- 3 LSB.

The DAC Current 12 bits supplies the sinus waveform between the – xVpk to xVpk. (x = 0.1 up to 1) via timing unit and wave table memory.
This Dac has a settling time min to max value of 35ns and a total precision of +/- 1.5 LSB.

The AOP converts the current output to voltage output with a settling time of 20ns.

To conclude we have a sinus waveform with 14 bits resolution on amplitude, and a precision < 1Hz on the frequency (sample rate 40Mhz).

The attenuator via sinus unit divides the amplitude sinus signal by step 1dB between 0dB to –62dB.
The link between the attenuator and the amplifier and the AOP is made by capacitor.
We have a mounted option to strap this attenuator to improve the sinus chain.
(Provided that EOS permits a sinus wave output amplitude between 0.565Vpeak to 5.65Vpeak).

4.8.2. Booster Unit

4.8.2.1.HARDWARE CHARACTERISTICS

Type of unit : Analogic.

Main components :

- Audio power amplifier. Ref: NS LM1876F.
- Lemo connector B series. Ref: EPG.00.302.NLN.

Power : +12V, -12V.

Consumption : +12V: 1,41Apeak.
-12V: 1,41Apeak.

Schematic : Eg. Annexe n° 1 p55.

4.8.2.2. FEATURES

This component is the booster of the sinusoid to give the power amplifier.

To answer at EOS requirements :

- 4 W / 4Ohms.
- Bandwith 500Hz-9Khz –3dB.
- THD <= 5% at max power.

The bandwith and the total harmonic distorsion is ensured by the specification component.
We adjust the bandwith by external component (dedicated capacitor).
For exemple, in the graph typical performance 15W on 4ohms gives a THD < 0.1%.

To obtain 4W on 4 Ohms we have a Vpeak = 5.656V, we adjust by external components the Gain of the amplifier.
We put a gain of 5.65 with precision (=0.1%) resistors that permits an voltage input of 1Vpeak max.

To improve the power dissipation, we need an heat sink > 13° c/W.

At max power, we need 1.41Apeak on the +12V and –12V line power.
The VME request is 1.5A in permanent state on these line powers.
To improve the EMC, we have implanted high charge capacitors with low ESR on the +12V and -12V line power near the amplifier component.

The link between the amplifier and the membrane mirror is actually direct.
We have implanted a mounted option to have a capacitor link (4700 µF).

The Lemo connector uses a push-pull self latching connection system, the current max is 2A.
This connector has two contacts, we have a mounted option to put the analogical ground on the second contact.

4.9. Power Unit

4.9.1. Hardware characteristics

Type of unit : Power.

Main components :

- Positive regulator voltage 500mA. Ref: ON MC78M05BDT.
- Negative regulator voltage 500mA. Ref: ON MC79M05BDT.

- Low drop out voltage 1.5A. Ref: MIC29150-33BU.

Power : +5Volts, +12Volts, -12Volts.

Consumption : +5V : 20mA.
+12V : 20mA.
-12V : 20mA.

Schematic : Eg. Annexe n° 1 p47 & p54 .

4.9.2. Features

We use a low drop out voltage to provide a 3.3 voltage for the FPGA components.

We use a positive voltage regulator to provide the +5 analogic voltage réference for the DAC components and discreet AOP (on the +12V line of VME interface).

We use a negative voltage regulator to provide the -5 analogic voltage réference for the DAC components and discreet AOP (on the -12V line of VME interface).

We implant fuses and EMI filter on each power lines.

The calcul of power dissipation on each regulator proves that we do not require special heat sink.

4.10. Oscillator

4.10.1.Hardware characteristics

Type of unit : Numeric (TTL).

Components :
- Oscillator 40Mhz. Ref: IQD IQXO-70-40Mhz.
- Skew clock driver. Ref: NS CGS74B2525M.

Power : +5Volts.

Consumption : 40mA.

Schematic : Eg. Annexe n° 1 p56.

4.10.2.Features

This oscillator supplies the basic clock 40Mhz.

5. SOFTWARE DESCRIPTION

The board describe in this document is provided with a software library that has the purpose of simplifying the board control for ESO developers.
This chapter describes on one hand the low level interfaces with the board itself and on the other hand the high level interfaces with software running on CPU.

5.1. Overview

To help the reader to understand this chapter we shortly recall the functionalities provided by this board to the user and also the main hardware components to configure.

The hardware solution design to answer to these requirements is composed of :

- one programmable memory which allows the user to define the pattern and the frequency of the modulation signal (bit 11 to 0) and to define the square wave counter A and B (bit 15 and 14).
  (a second table identical to this one allows to switch in real time between two frequency for tuning purpose).
- one programmable 12 bits converter which allows to generate a sinusoid with an amplitude between 0,1 and 1 Volt Peak. To define the amplitude we use a programmable reference voltage which allow to cover the dynamic range (0,1 to 1 Volt) with an accuracy 16 bit.
- one programmable attenuator which could be used if the required amplitude is smaller than 0,1 Volt. This component is placed after the 12 bits converter.
- One booster to amplify the signal by a factor of 5,65.
- One interlock system.

5.2. Software environment

The LCU software environment consists in :

- Tornado operating system,
- LCU Common Software (LCC).

5.3. Hardware environment

The main hardware elements of the MACAO RTC are :

- 1 PowerPC board as Supervisor (LCU),
- 1 PowerPC board as Real Time computer,
- 1 APD counters board (SHAKTIWARE),
- 1 TIM board,
- 1 MAC4 board,
- 1 VME4SA board,
- 1 ACRO9481 board,
- VMIVME5576 board,

5.4. Standard

The standard prescribed by the “VLT Software, Programming Standards” and guidelines described in “Guidelines for the development of VLT Application Software” are applied.

5.5. Interfaces

5.5.1. high-level interfaces : interfaces with ESO software running on PowerPC

General rules for return codes:

- If the command doesn't return data, it returns just a status code. The value 0 always means OK and a negative number encodes an error. Don't use positive numbers.
- If the command returns data, these should be positive. A negative number encodes the error.

The high level functions are coded in acbHighLevel.c. We give hereafter an exhaustive list of the exported functions (to be validate by ESO) :

Names	Description	return value
Int acbInit	Board initialization after power-up to check that the board is accessible.	0: ok -1 : board not present
Int acbShutdown	Reverse of acbInit. Prepare the board to power off. (switch off the signal outputs)	0: ok -1 : failure
Int acbSelfTest (int test)	Board test : this function invoke the self test facilities which are programmed into the board.The parameter 'test' could be : ACB_TEST_PROBE : controls that the board is accessible ACB_TEST_MEMORY : tests all the memories in read/write access ACB_TEST_REGISTER : tests all the registers ACB_TEST_COUNT : checks that the test counter run correctly ACB_TEST_SINUS : generates a sinusoid with a pre-define characteristics during one minute (to be confirmed by ESO) ACB_TEST_ALL : runs all the tests excepted SINUS	0: ok -1 : failure for PROBE -2 : failure for MEMORY -3 : failure for REGISTER -4 : failure for COUNT a more detailed description will be define during test.

Names	Description	Return value
int acbSimulate (int command,int section)	The command could be: ACB_SIM_START ACB_SIM_STOP ACB_SIM_STATUS The first two with obvious meaning, while the third one asks for the status of the simulation, if it is on or off. Section determine the type of simulation : ACB_SIM_ FULL_SOFT : with don't access to the board and we apply the code to a full-software board. ACB_SIM_ COUNT : we don't read the count value on board but on a pre-define table. In this case we deal with the interrupt and we have the real timing of the board. ACB_SIM_ SINUS : we don't activate the sinus output. ACB_SIM_ ALL : ACB_SIM_ SINUS and ACB_SIM_ COUNT	For command START and STOP: 0: ok -1 : failure For command STATUS: A number >=0 is the status, the possible values are : ACB_SIM_ON ACB_SIM_OFF A negative number encoding the failure reason in case of error.
int acbSetFrequency(double frq)	Set the base frequency of the sinusoid and the square wave. Parameter ' frq' is the frequency in Hertz. This function take 35 ms to load the new sinusoid pattern and after switch from one table to the other one between to frame.	0: ok -1 : error
int acbSetPhaseDelay(double phase)	Set the phase shift: this function will set the phase delay between the sinusoid and the square wave. IMPORTANT: The sinusoid is the reference and square wave that drives the counters is the slave. This is the wave delayed by this parameter. A negative delay is a phase anticipation. Parameter ' phase' is the phase delay in radians.	0: ok -1 : error

Names	Description	Return value
int acbTransferIRQEnable(int IRQnumber, FUNCPTR routine, int arg)	Enables IRQ transfer generated after each frame reception. An interrupt should be generated at the end of each transfer: the address of the ISR is provided (parameter 'routine' and 'arg'). The IRQ number is given by user.	0: ok -1 : error
int acbGetBlockTransferSize(int flag)	Returns the width of a single BLT transfer in byte. The BLT frame is limited to 256 bytes. We have 60*2 counts 2 bytes each + 2 bytes test counter + 2 bytes heartbeat for count A + 2 bytes test counter + 2 bytes heartbeat for count AB This value will be used to allocate memory for the transfer block. If 'flag'!=0 include also the heartbeat and the test counter in the computation.	The number of bytes to allocate for a subsequent BLT transfer. Flag = 0 return value is 240 bytes Flag = 1 return value is 248 bytes A negative number encoding the failure reason in case of error.
int acbGetFrameBLT(void* buffer ,int flag)	Reads a frame of counter values directly through the VME bus into 'buffer' in BLT mode. The size of the buffer was previously computed with acbGetBlockTransferSize. Option: include also the heartbeat with 'flag' != 0.	0: ok -1 : failure
int acbTransferIRQDisable()	Disables the generation of one IRQ after the reception of one frame.	0: ok -1 : failure
int acbGetFrame(void* buffer ,int flag)	Reads a frame of counter values directly through the VME bus into 'buffer'. The size of the buffer was previously computed with acbGetBlockTransferSize. Option: include also the heartbeat with 'flag' != 0.	0: ok -1 : failure

Names	Description	Return value
int acbSetAmplitude(double amplitude	Sets the amplitude: this function will set the amplitude of the sinusoid. This function takes ?? ms and it could be called during closed loop operation in real time mode. Parameter 'amplitude' ranges from 0 to 1 where 0 is voltage=0 and 1 is the maximum. (5,65 Volt)	0: ok -1 : failure
int acbSetInterlockStatus (int status)	Set interlock: this function enables the interlock after power on or disable it causing the APDs to switch OFF. The parameter 'status' can be: ACB_INTERLOCK_ON ACB_INTERLOCK_OFF	A number >= 0 is the status, table to be provided A negative number encoding the failure reason in case of error.
int acbInterlockIRQEnable(int IRQnumber, FUNCPTR routine, int arg)	Enables Interlock IRQ generatedthe interlock system detect one saturation. The address of the ISR is provided (parameter 'routine' and 'arg'). The IRQ number is given by user.	0: ok -1 : error
int acbGetInterlockStatus (void)	Get interlock status	A number >= 0 is the status, table to be provided. Something as: ACB_INTERLOCK_ON ACB_INTERLOCK_OFF ACB_INTERLOCK_NOTACTIVE A negative number encoding the failure reason in case of error.
int acInterlockIRQDisable()	Disables the generation of one IRQ after one saturation detection by interlock system.	0: ok -1 : failure

Names	Description	Return value
int acbSetInterlockThreshold(unsigned short threshold)	Set interlock threshold. This threshold defines when an overcount occurs. In this case the interlock will change to OFF state switching off the APDs. Threshold is given in counts per second and is converted in frame counts according to sinusoid frequency in the function.	A number >= 0 is the status, table to be provided A negative number encoding the failure reason in case of error.

The values of :
ACB_SIM_START
ACB_SIM_STOP
ACB_SIM_STATUS
ACB_SIM_ON
ACB_SIM_OFF
ACB_SIM_ FULL_SOFT
ACB_SIM_ COUNT
ACB_SIM_ SINUS
ACB_SIM_ ALL
ACB_TEST_PROBE
ACB_TEST_MEMORY
ACB_TEST_REGISTER
ACB_TEST_COUNT
ACB_TEST_SINUS
ACB_TEST_ALL
ACB_INTERLOCK_ON
ACB_INTERLOCK_OFF
ACB_INTERLOCK_NOTACTIVE
Will be define in ApdCounterHighLevel.h. The functions prototypes will also be define in this file.

5.5.2. Low-level interfaces : interfaces with SHAKTIWARE board

5.5.2.1. BOARD ACCESS

To access to the Shaktiware board we use standard VME access mode excepted for the counter table which is read in BLT mode.
The board is seen from the CPU as a structure composed of memory and registers map in the base address of the board.
The struct of this board is given hereafter.

```
struct acbBoard
{
        short int table1[0x8000] ;      /* 16 bits memory (read/write) accessible */
        short int nothing0[0x8000] ;    /* 16 bits memory (read/write) accessible */
        short int table2[0x8000] ;      /* 16 bits memory (read/write) accessible */
        short int nothing1[0x8000] ;    /* 16 bits memory (read/write) accessible */
        int dpram[61] ;                 /* 32 bits memory (read) accessible in BLT mode */
        int nothing2[0x8000 - 61] ; /* 32 bits memory no available (only for mapping) */
        short int interlock_data ;      /* 16 bits register (read/write) accessible */
        short int amplitude_data ;      /* 16 bits register (read/write) accessible */
        short int attenuator_data ;     /* 16 bits register (read/write) accessible */
        short int reserved0 ;           /* 16 bits register (read/write) accessible */
        short int countA_data ;         /* 16 bits register (read/write) accessible */
        short int countB_data ;         /* 16 bits register (read/write) accessible */
        short int APDpulse_data ;       /* 16 bits register (read/write) accessible */
        short int table1_count_data ; /* 16 bits register (read/write) accessible */
        short int table2_count_data ; /* 16 bits register (read/write) accessible */
        short int nothing3[0x10000 - 9] ;/* 32 bits memory no available (only for
mapping) */
        short int interlock_system ;    /* 16 bits register (read/write) accessible */
        short int amplitude_system ; /* 16 bits register (read/write) accessible */
        short int attenuator_system ; /* 16 bits register (read/write) accessible */
        short int sinus_system ;        /* 16 bits register (read/write) accessible */
        short int count_system ;        /* 16 bits register (read/write) accessible */
        short int reserved1 ;           /* 16 bits register (read/write) accessible */
        short int APDpulse_system ; /* 16 bits register (read/write) accessible */
        short int IT_system ;           /* 16 bits register (read/write) accessible */
};
```

5.5.2.2. BOARD ONFIGURATION

To configure the board we use register “xxx_data” to set the value and we write in “xxx_system” register to apply the value to the current configuration. Then we read “xxx_system” register to control that the the requested action is apply.

5.6. Implementation break-down

5.6.1. AcbHighLevel

5.6.1.1. ACBINIT

Input : none
Output : Ok or error
Error : see below
Pseudo-code :
Read the physical address associated to board
Translate this address by use of **BusToLocalAdrs**
Test if the board if accessible
If the board is not here set variable **staticBoardPt** to NULL else to the right value
(staticBoardPt is a variable static to the module AcbDrv)
Called function :
BusToLocalAdrs

5.6.1.2. ACBSHUTDOWN

Input : none
Output : Ok or error
Error : see below
Pseudo-code :
Close the sinusoid output
Shut-down the booster
Shut-down the 12 bits converters
Set staticBoardPt to NULL (staticBoardPt is a variable static to the module AcbDrv)
Called functions :
AcbdrvBooster (OFF)
AcbdrvCDA (OFF)
AcbdrvOutput (OFF)

5.6.1.3. ACBSELFTEST

Input : test number
Output : Ok or error
Error : see below
Pseudo-code :
PROBE :
Test that the board is accessible
MEMORY :
Use **AcbdrvTstData** and **AcbdrvTstAddress** to control the memory bank of the board

REGISTER :

Use **AcbdrvWriteDataRegister** and **AcbdrvReadDataRegister** to control the data registers

Use **AcbdrvWriteSystemRegister** and **AcbdrvReadSystemRegister** to control the system registers

COUNT :

Configure and load a pre-define sinusoid (frequency,amplitude) with **AcbdrvCreateConfig** and **AcbdrvLoadConfig**, configure the test counter with **AcbdrvCountTestConfig**, read the receive data by test counter with **AcbdrvReadCounters** and check the correctness of the value

SINUS :

Configure and load a pre-define sinusoid (frequency,amplitude) with **AcbdrvCreateConfig** and **AcbdrvLoadConfig**, run during 1 minute and then close the signal output with **AcbdrvOutput**

ALL :

Run all functions excepted SINUS and COUNT

Called functions :

AcbdrvTstData (bankPt, sizeOfbank, typeOfbank)
AcbdrvTstAddress (bankPt, sizeOfbank, typeOfbank)
AcbdrvWriteDataRegister (registerNumber, Value)
AcbdrvReadDataRegister (registerNumber, &Value)
AcbdrvWriteSystemRegister (registerNumber, Value)
AcbdrvReadSystemRegister (registerNumber, &Value)
AcbdrvCreateConfig
AcbdrvLoadConfig
AcbdrvCountTestConfig
AcbdrvReadCounters
AcbdrvOutput

5.6.1.4.ACBSIMULATE

Input : int command,int section
Output : Ok or error
Error : see below
Pseudo-code :

ACB_SIM_START :

Start simulation according to section

ACB_SIM_STOP :

Stop simulation

ACB_SIM_STATUS :

Read simulation status

Section :

ACB_SIM_FULL_SOFT :

Allocate memory on CPU and set staticBoardPt to the allocated memory.

Set **staticSimulationSoftStatus** to ON.

This integer static to the module acbdrv is use in functions which read status register, in fact with this type of simulation the bit of status register don't change.

ACB_SIM_COUNT :

Set **staticSimulationCountStatus** to ON.

This integer static to the module acbdrv is use in function **AcbdrvReadCounters** which reads counter value. If the flag is ON the values are read in a pre-define table

ACB_SIM_SINUS :

close the signal output with **AcbdrvOutput**

Called functions :

AcbdrvOutput
AcbdrvReadCounters

5.6.1.5.ACBSETFREQUENCY

Input : double frequency
Output : Ok or error
Error : see below
Pseudo-code :

Read the table currently used.
Define the value to load in table for this frequency
Set the **staticFrequencyValue** This double static to the module acbdrv is use in functions which need to know the frequency.
Load the value in the other table
Switch on the new table

Called function :

AcbdrvSetConfig
AcbdrvLoadConfig

5.6.1.6.ACBSETPHASEDELAY

Input : double phase
Output : Ok or error
Error : see below
Pseudo-code :

Read the frequency currently used
Read the number of point in sinusoid
Convert the phase in radian to a value in tick of 25 ns

Called function :

AcbdrvSetShift

5.6.1.7.ACBTRANSFERIRQENABLE

Input : int IRQnumber, FUNCPTR routine, int arg
Output : Ok or error
Error : see below
Pseudo-code :
Enable Transfer interrupt
Called functions :
acbSetInterlockIRQ

5.6.1.8.ACBGETBLOCKTRANSFERSIZE

Input : int flag
Output : Ok or error
Error : see below
Pseudo-code :
Define the number of bytes to transmit from SHAKTIWARE board to PowerPC board (240 bytes if flag is set to 0 and 248 if flag is set to 1)
Called functions :

5.6.1.9.ACBGETFRAMEBLT

Input : void* buffer, int flag
Output : Ok or error
Error : see below
Pseudo-code :
Determine the number of byte to read by using AcbGetBlockTransferSize
Read the count values in one frame in BLT mode
To be sure that all the counter are from the same frame this function has to be called after each TransferIRQ reception. An other solution is to measure the current time on IRQ reception and at the end of the transfer and to control that the delay is inferior to a period.
Called functions :
AcbdrvBLTReadCounters
AcbGetBlockTransferSize

5.6.1.10.ACBTRANSFERIRQDISABLE

Input : none
Output : Ok or error
Error : see below
Pseudo-code :
Disable Transfer IRQ
Called functions :
acbSeTransferIRQ

5.6.1.11.ACBGETFRAME

Input : void* buffer, int flag
Output : Ok or error
Error : see below
Pseudo-code :

Determine the number of byte to read by using AcbGetBlockTransferSize
Read the count values in one frame
To be sure that all the counter are from the same frame this function has to be called after each TransferIRQ reception. An other solution is to measure the current time on IRQ reception and at the end of the transfer and to control that the delay is inferior to a period.
We could also read the frame counter number before reading the counter values and after. We can control the frame number is always the same after the reading of values.

Called functions :

AcbGetBlockTransferSize
AcbdrvBLTReadCounters

5.6.1.12.ACBSETAMPLITUDE

Input : double amplitude
Output : Ok or error
Error : see below
Pseudo-code :

Convert amplitude in Volt :
0 => 0
1 => 5,65 V
If VoltAmplitude is greater than 0,6 V then set directly the amplitude value **acbdrvSetAmplitude**
Else
Set the attenuator value **acbdrvSetAttenuator** to reduce the amplitude in a correct range and then define exactly the amplitude value with **acbdrvSetAmplitude**

Called functions :

acbdrvSetAmplitude
acbdrvSetAttenuator

5.6.1.13.ACBGETINTERLOCKSTATUS

Input : none
Output : Ok or error
Error : see below
Pseudo-code :

Read Interlock status in staticInterlockStatus, if Interlock system is ON, read Interlock current statud with **acbdrvGetInterlockStatus**

Called functions :

acbdrvGetInterlockStatus

5.6.1.14. ACBSETINTERLOCKSTATUS

Input : status
Output : Ok or error
Error : see below
Pseudo-code :

ACB_INTERLOCK_ON :

Set interlock register
B0 : 0 => interlock active
B1 : 1 => Led interlock enable : 0 => Led interlock disable

ACB_INTERLOCK_OFF :

Set interlock register
B0 : 1 => counter reset to 0
B1 : 1 => Led interlock enable : 0 => Led interlock disable

TBD by ESO

set **staticInterlockStatus** to the apply value

Called functions :

acbSetInterlockIRQ

5.6.1.15. ACBSETINTERLOCKTHRESHOLD

Input : unsigned short threshold
Output : Ok or error
Error : see below
Pseudo-code :

Read the current frequency
Translate the threshold in count per second in a value in count per frame
If the number of count per second for one counter is greater as the threshold the interlock will change to OFF state and the APDs are switch off

Called functions :

acbdrvSetInterlockThreshold

5.6.2. ApdLowLevel

5.6.2.1. STATIC VARIABLE

StaticBoardPt
StaticNumberofBytes
staticSimulationCountStatus
StaticFrequencyValue
staticSimulationSoftStatus
StaticInterlockStatus

5.6.2.2. LOW LEVEL FUNCTIONS

AcbdrvWriteDataRegister (registerNumber, Value)
AcbdrvReadDataRegister (registerNumber, &Value)
AcbdrvWriteSystemRegister (registerNumber, Value)
AcbdrvReadSystemRegister (registerNumber, &Value)
AcbdrvBooster
AcbdrvCDA
AcbdrvOutput
AcbdrvSetShift
acbdrvSetAmplitude
acbdrvSetAttenuator
acbdrvSetInterlockThreshold
acbdrvSetInterlockStatus
acbdrvGetInterlockStatus
acbdrvSetInterlockIRQ
acbdrvSetTransferIRQ

AcbdrvReadCounters
AcbdrvBLTReadCounters

AcbdrvTstData (bankPt, sizeOfbank, typeOfbank)
AcbdrvTstAddress (bankPt, sizeOfbank, typeOfbank)
AcbdrvCreateConfig
AcbdrvSetConfig
AcbdrvLoadConfig
AcbdrvCountTestConfig

6. ELECTRICAL AND ENVIRONMENTAL REQUIREMENTS

6.1. Technology

6.1.1. Components

The components are choosen in industrial version - 55° C, +70 ° C. They are mainly in SMC.
The PROM for first FPGA is mounted on support.

6.1.2. Printed Board

The printed circuit is achieved in multilayered on substratum Epoxy. It includes two layers for power and ground and six signal layers.
A signal segregation is made in inserting power and ground plan between signal layers.
The name of component are silk-screen printing.

6.2. Power consumption

The board respects the VMEbus specification.
The consumption is evaluated at :

- +5 Volts : 1.8A permanent – 2.5A peak.
- +12 Volts : 1.42Apeak.
- -12 Volts : 1.42Apeak.

These evaluations will be confirmed by tests.

6.3. Environmental specifications

Functional air temperature range : -10° C to +30° C.
Typical air temperature gradient : 0.4° C/hour.
Operational altitude : 0m to 2800m.

6.4. EMI/EMC features

In order to have a reliable computer in harsh environment and in order to guarantee electromagnetic compatibility, the following rules have been applied.

1. The conception and the routing of the boards has been done as following:
   - Decoupling for each active component <1mm,
   - Multilayer, ground and power planes,
   - Supply filtering,
   - SMC components,
   - Clock path optimized and shielded,
   - Synchronous logic.

2. An EMI filter has been implemented on the power line inputs.

3. In order to prevent an electronics system composed of many different components from EMI/EMC, the optimal solution is that each cabinets, each grounded back planes and each platings are linked each other by the more connecting points as possible. This ground mesh is the only valuable protection against HF disturbances and will be implemented.

4. The system subracks meet the standard of interference emission EN 50081-1 and the standard of susceptibility EN 50 082 -2.

We have implanted some hardware mounted options (ESD capacitor) on the APD signals.

For the components in contact with exterior signals (eg. VME bus, Interlock, …), we have chosen these components in relation with their availability to answer at EMC/ESD requirements (eg. ABT logical component 2KV ESD).

7. MECHANICAL REQUIREMENTS

7.1. Form factor

The board is a double europe board factor.

In the rear board, we use the P1 and P2 connectors.

- Count_A signal : P2C1,
- Count_B signal : P2C2,

In the front board we have :

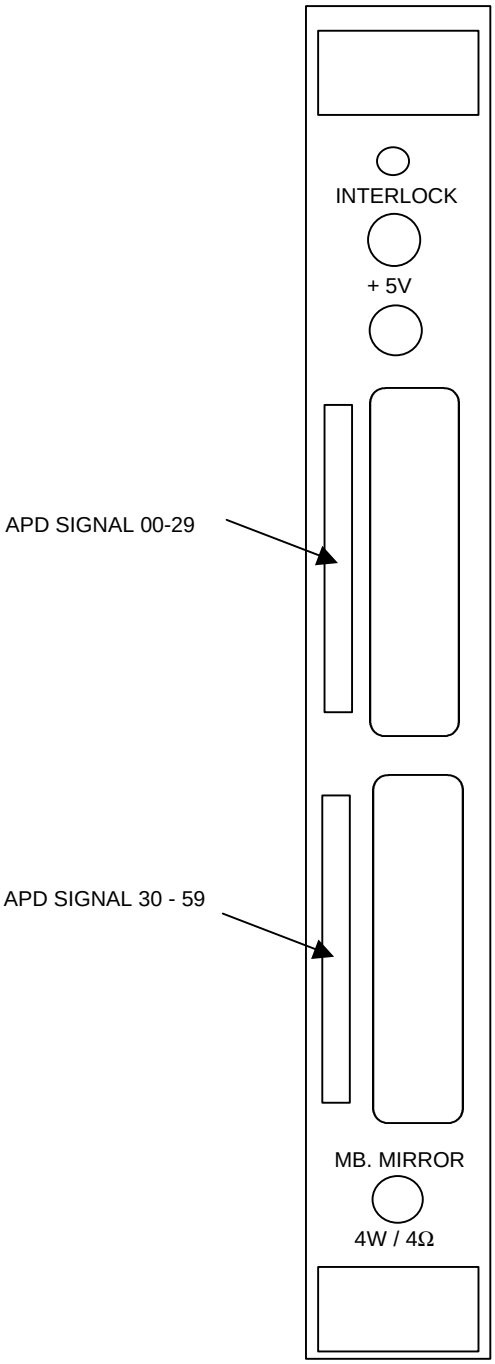
- two SMC connectors for interlock relay,
- one LEMO connector for the membrane mirror,
- one led for presence interlock,
- two SCSI connectors.

7.2. Unit identification label

Each unit will be identified with the following informations :

- Unit name,
- Unit serial number,
- Manufacturer,
- Manufacturing date,
- Power suppy voltage, frequency and current,
- Shaktiware logo.

7.3. Mechanical Overview Drawing



8. MAINTENANCE AND TESTS FACILITIES

8.1. ACM maintenance concept

The ACM that we propose is composed of only one unit which can be considered as an LRU (Line replaceable Unit).
An intervention on a LRU does not require its removal from its working environment or the removal of another LRU. Tests on LRU can be achieved at the working site, and do not require the use of specific tools.

8.2. Plug 'n' Play

It will be possible to replace any board without re-calibration or board configuration (except : board address coding).

8.3. Test Points

Test points will be provided on this board to ease the tests and the maintenance procedures :

- APD signal inputs,
- timing unit signals,
- membrane output before amplifier,
- membrane output after amplifier,
- interlock signal.

LEDs:

- two led for the loading FPGA state,

8.4. Maintenance Operations

For ALL OPERATIONS ON THE ACM, beware of static discharges. Technicians must wear grounded bracelet. Anti-static flooring under the LRU would be a plus.

Check that the board is well seated.

Power supply test: the aim of this test is to plug the board when the rack is off and then turn the power on and check the Power Supply LED status. This test requires no other module.

Loading test: The aim of this test is to verify the status of the FPGA loading by following the loading flag. This test requires no other module.

I/O test: The aim of this test is to make a read/write test sequence between the VME bus and the control register to check the read and written values. This test requires no other module.

Memories test: The aim of this test is to access all memory banks of the ACM through the VME bus and then to achieve a read/write test sequence. This test requires no other module.

Pulse test: The aim of this test is to verify the count pulse rate by loading a deterministic APD signal and reading the count value. This test requires no other module.

Sinus wave test: The aim of this test is to check the output signals of the Timing unit with an oscilloscope. This test requires no other module.

Interlock test: The aim of this test is to check the interlock signal with an oscilloscope by loading a deterministic APD signal. This test requires no other module.

Track test: The aim of this test is to check the continuity of the different bus tracks. It consists in checking the resistivity between two equivalent pins of different connectors with an ohmmeter.

8.5. Self-Tests

Operation	Analysis and results
Verify status FPGA loading	FPGA programming
Read/write test sequence in the controle register	RTC interface unit working
Read/write test sequence in the memory banks	Memories working
Load a deterministic APD signal	Counter unit and timing unit working

8.6. Monitoring

For monitoring purpose, we add a supplementary input for ACM with a programmable deterministic value pulse generator.
It allows to control that the ACM performs correctly and it could be used by the RTC to implement a real time monitoring of the loop.

9. DOCUMENTATION

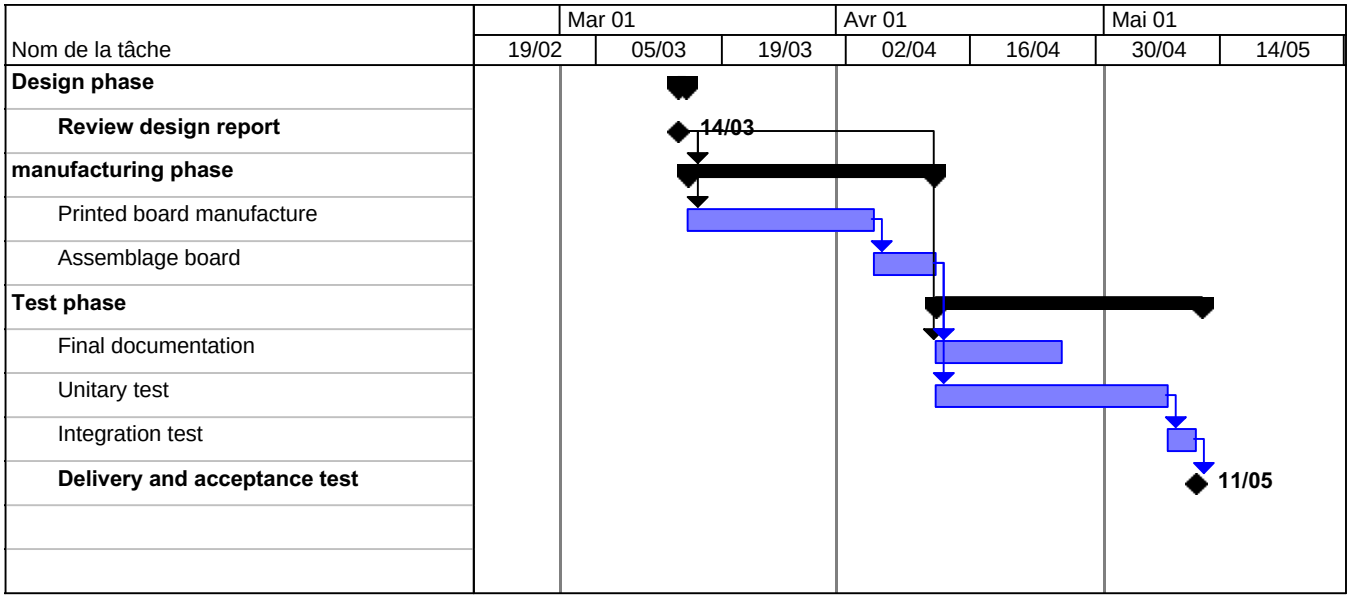
The following documentation will be delivered with each APD counter module :
1. Users manual,
2. Installation manual,
3. Maintenance and troubleshooting manual,
4. Acceptance test protocol.

The following documentation will be delivered with the first APD counter module :
5. Schematics for all boards,
6. Backplane protocol description.

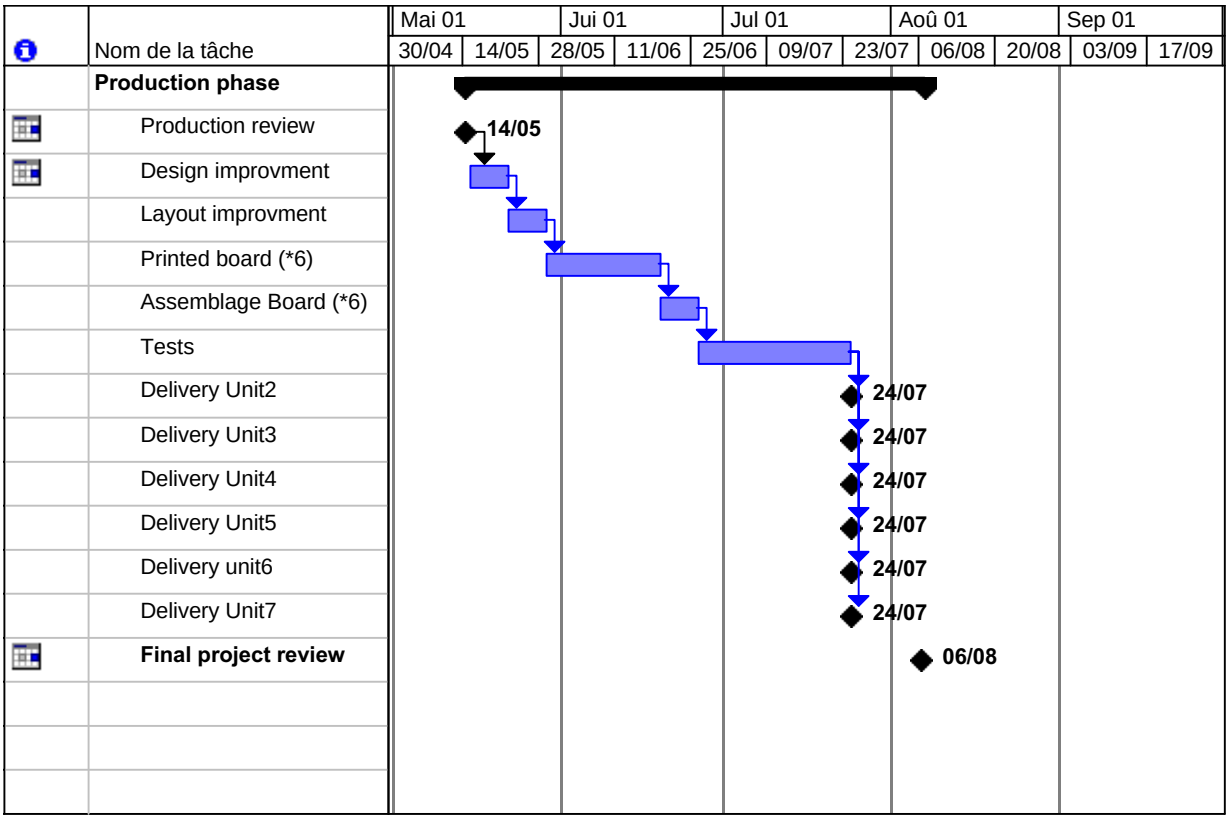
All documentation will be in English. In addition to paper documentation we will provide the electronic version. All the documentation will be provided with the first system.

10. PLANNING

10.1. Development planning



10.2. Production planning



11. ACCEPTANCE

An acceptance test document will formalize tests to achieve and will be approved after the design report review.
These following tests are provided as an example.

11.1. Unitary tests

Every function of the library will be indidually tested.

11.2. Validation tests

Measurement of power consumption.
Test of each APD counter.
Test of linearity on one APD counter.
Test of the interlock system.
Test of sinus wave with multifrequency.
Test of the power amplifier.
Test of the resolution on amplitude, frequency and phase.
Test of the system in saturation mode (without interlock).
Test of the system in low flux mode (we only send some trigger).
Test of the system without flux during one hour
Test of the monitoring counter for 24 hours.

11.3. Integration tests

These tests will be made at ESO.

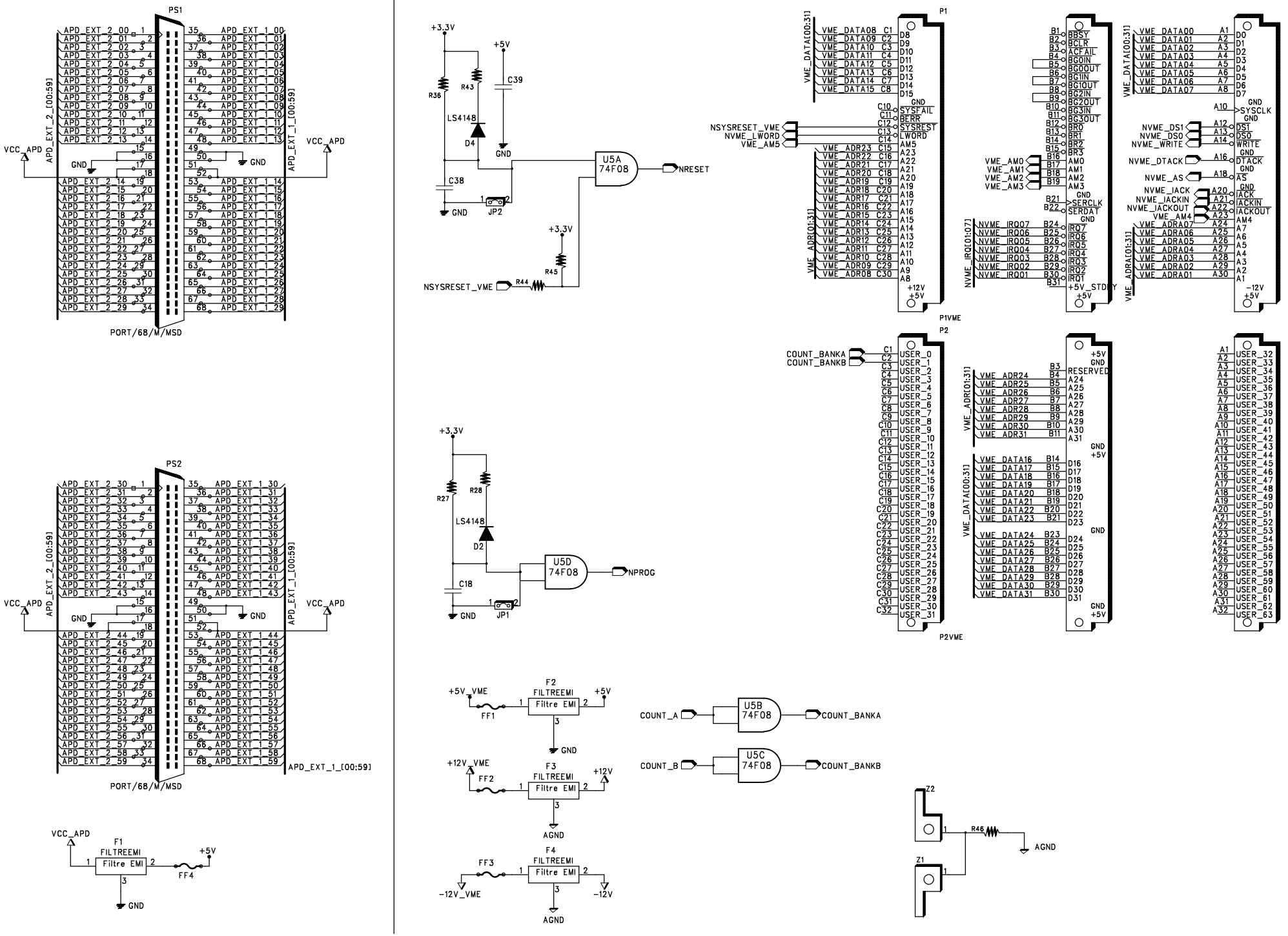
11.4. Test tools

Pulse generator.

11.5. Factory Support Equipment

We need an APD simulator.
We need a computer with VxWork software.

12. ANNEXES 1 ELECTRONICS SCHEMATICS


PS1
APD_EXT_2_00
APD_EXT_2_01
APD_EXT_2_02
APD_EXT_2_03
APD_EXT_2_04
APD_EXT_2_05
APD_EXT_2_06
APD_EXT_2_07
APD_EXT_2_08
APD_EXT_2_09
APD_EXT_2_10
APD_EXT_2_11
APD_EXT_2_12
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APD_EXT_2_20
APD_EXT_2_21
APD_EXT_2_22
APD_EXT_2_23
APD_EXT_2_24
APD_EXT_2_25
APD_EXT_2_26
APD_EXT_2_27
APD_EXT_2_28
APD_EXT_2_29
APD_EXT_2_[00:59]
APD_EXT_1_00
APD_EXT_1_01
APD_EXT_1_02
APD_EXT_1_03
APD_EXT_1_04
APD_EXT_1_05
APD_EXT_1_06
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APD_EXT_1_25
APD_EXT_1_26
APD_EXT_1_27
APD_EXT_1_28
APD_EXT_1_29
APD_EXT_1_[00:59]
VCC_APD
GND
PORT/68/M/MSD
PS2
APD_EXT_2_30
APD_EXT_2_31
APD_EXT_2_32
APD_EXT_2_33
APD_EXT_2_34
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APD_EXT_1_51
APD_EXT_1_52
APD_EXT_1_53
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APD_EXT_1_55
APD_EXT_1_56
APD_EXT_1_57
APD_EXT_1_58
APD_EXT_1_59
F1
FILTREEMI
Filtre EMI
+5V
FF4
+3.3V
+5V
R43
R38
C39
LS4148
D4
C38
JP2
U5A
74F08
NRESET
R45
R44
NSYSRESET_VME
R27
R28
D2
C18
JP1
U5D
NPROG
F2
FF1
F3
FF2
F4
FF3
+12V_VME
-12V_VME
AGND
-12V
U5B
U5C
COUNT_A
COUNT_B
COUNT_BANKA
COUNT_BANKB
P1
P1VME
VME_DATA[00:31]
VME_DATA08
VME_DATA09
VME_DATA10
VME_DATA11
VME_DATA12
VME_DATA13
VME_DATA14
VME_DATA15
SYSFAIL
BERR
SYSRESET
LWORD
VME_AM5
VME_ADR23
VME_ADR22
VME_ADR21
VME_ADR20
VME_ADR19
VME_ADR18
VME_ADR17
VME_ADR16
VME_ADR15
VME_ADR14
VME_ADR13
VME_ADR12
VME_ADR11
VME_ADR10
VME_ADR09
VME_ADR08
VME_ADR[01:31]
+12V
BBSY
BCLR
ACFAIL
BG0IN
BG0OUT
BG1IN
BG1OUT
BG2IN
BG2OUT
BG3IN
BG3OUT
BR0
BR1
BR2
BR3
VME_AM0
VME_AM1
VME_AM2
VME_AM3
AM0
AM1
AM2
AM3
SERCLK
SERDAT
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
IRQ2
IRQ1
NVME_IRQ[01:07]
NVME_IRQ07
NVME_IRQ06
NVME_IRQ05
NVME_IRQ04
NVME_IRQ03
NVME_IRQ02
NVME_IRQ01
+5V_STDBY
SYSCLK
NVME_DS1
NVME_DS0
NVME_WRITE
NVME_DTACK
NVME_AS
NVME_IACK
NVME_IACKIN
NVME_IACKOUT
VME_AM4
VME_ADRA07
VME_ADRA06
VME_ADRA05
VME_ADRA04
VME_ADRA03
VME_ADRA02
VME_ADRA01
VME_ADRA[01:31]
P2
P2VME
COUNT_BANKA
COUNT_BANKB
USER_0
USER_1
USER_2
USER_3
USER_4
USER_5
USER_6
USER_7
USER_8
USER_9
USER_10
USER_11
USER_12
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USER_20
USER_21
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USER_50
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USER_54
USER_55
USER_56
USER_57
USER_58
USER_59
USER_60
USER_61
USER_62
USER_63
RESERVED
VME_ADR24
VME_ADR25
VME_ADR26
VME_ADR27
VME_ADR28
VME_ADR29
VME_ADR30
VME_ADR31
VME_DATA16
VME_DATA17
VME_DATA18
VME_DATA19
VME_DATA20
VME_DATA21
VME_DATA22
VME_DATA23
VME_DATA24
VME_DATA25
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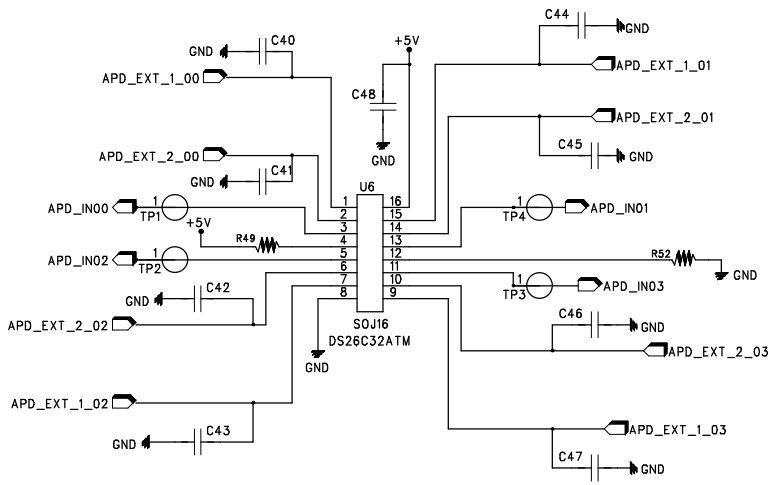
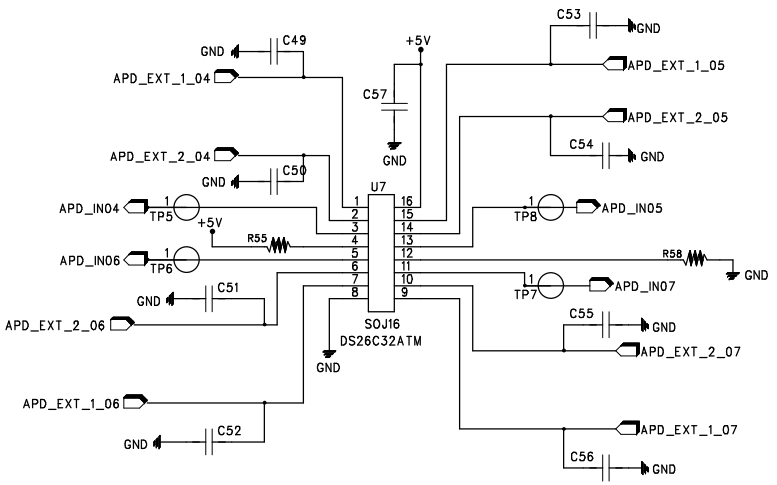
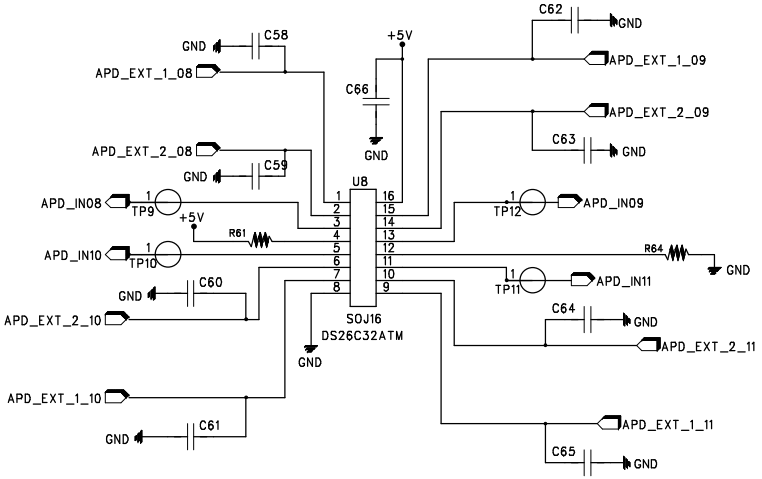
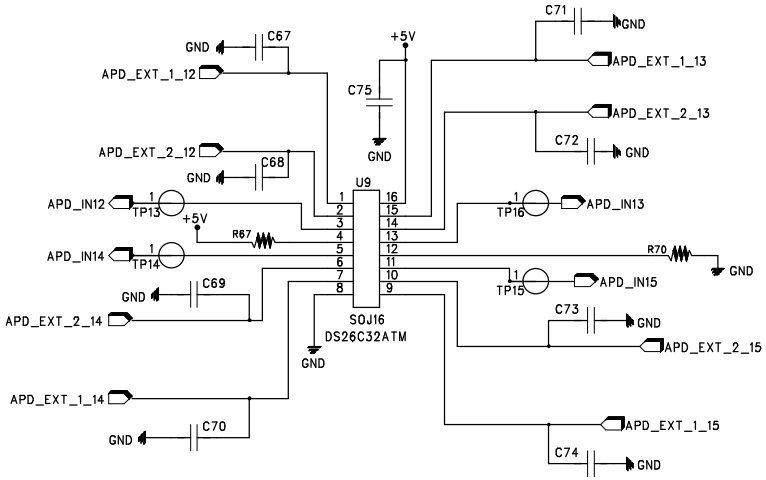
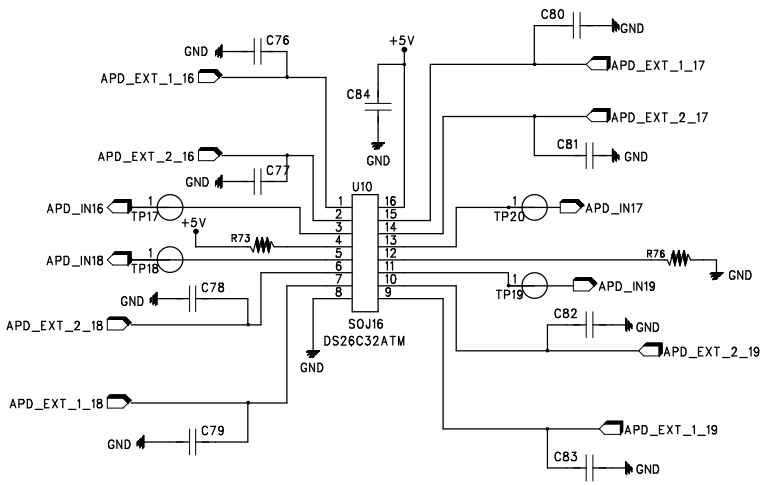
VME_DATA28
VME_DATA29
VME_DATA30
VME_DATA31
Z2
Z1
R46

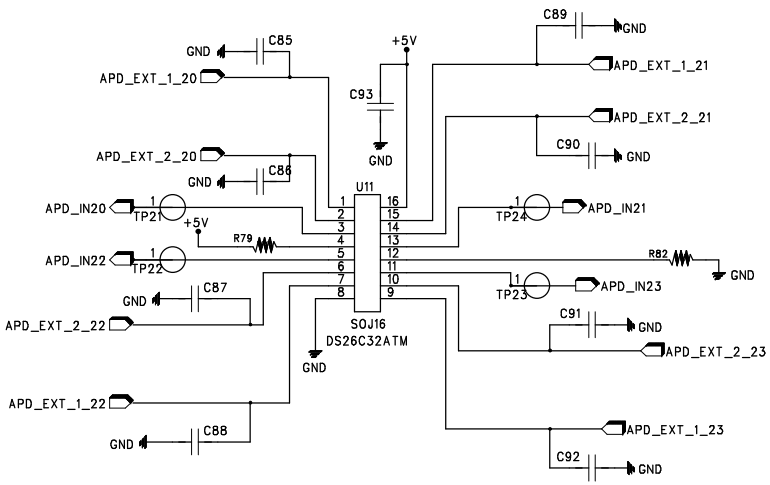

U6
SOJ16
DS26C32ATM
C40
C41
C42
C43
C44
C45
C46
C47
C48
R49
R52
TP1
TP2
TP3
TP4
+5V
GND
APD_EXT_1_00
APD_EXT_2_00
APD_IN00
APD_IN02
APD_EXT_2_02
APD_EXT_1_02
APD_EXT_1_01
APD_EXT_2_01
APD_IN01
APD_IN03
APD_EXT_2_03
APD_EXT_1_03

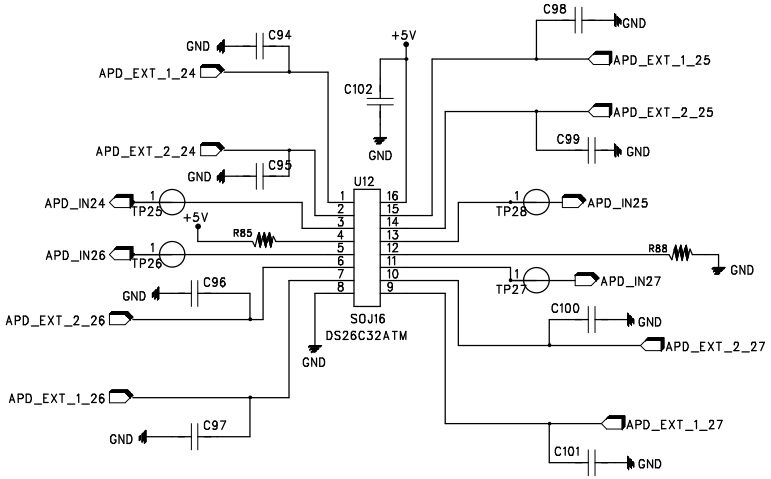

U7
SOJ16
DS26C32ATM
C49
C50
C51
C52
C53
C54
C55
C56
C57
R55
R58
TP5
TP6
TP7
TP8
+5V
GND
APD_EXT_1_04
APD_EXT_2_04
APD_IN04
APD_IN06
APD_EXT_2_06
APD_EXT_1_06
APD_EXT_1_05
APD_EXT_2_05
APD_IN05
APD_IN07
APD_EXT_2_07
APD_EXT_1_07

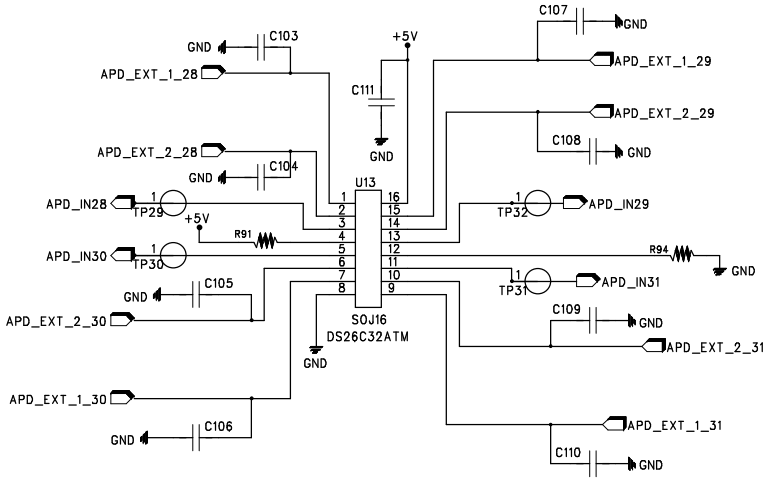

U8
SOJ16
DS26C32ATM
C58
C59
C60
C61
C62
C63
C64
C65
C66
R61
R64
TP9
TP10
TP11
TP12
+5V
GND
APD_EXT_1_08
APD_EXT_2_08
APD_IN08
APD_IN10
APD_EXT_2_10
APD_EXT_1_10
APD_EXT_1_09
APD_EXT_2_09
APD_IN09
APD_IN11
APD_EXT_2_11
APD_EXT_1_11

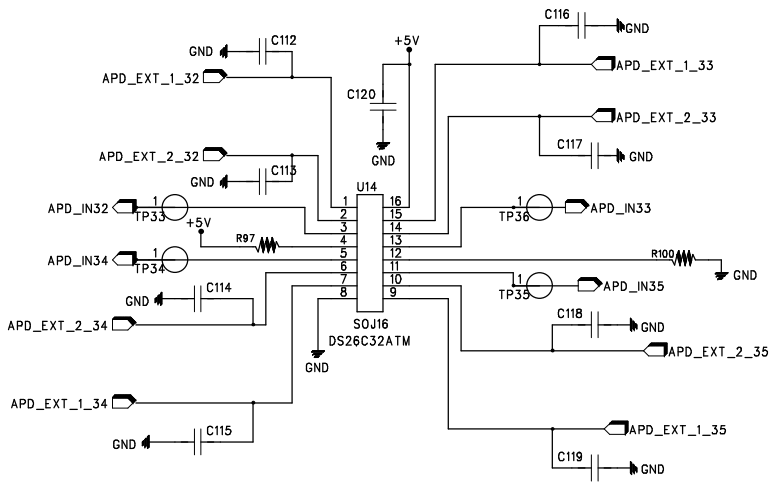

U9
SOJ16
DS26C32ATM
C67
C68
C69
C70
C71
C72
C73
C74
C75
R67
R70
TP13
TP14
TP15
TP16
+5V
GND
APD_EXT_1_12
APD_EXT_2_12
APD_IN12
APD_IN14
APD_EXT_2_14
APD_EXT_1_14
APD_EXT_1_13
APD_EXT_2_13
APD_IN13
APD_IN15
APD_EXT_2_15
APD_EXT_1_15

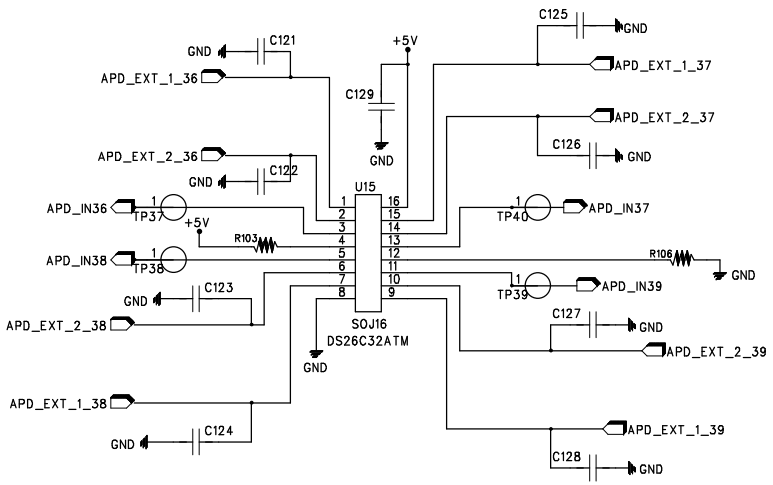

U10
SOJ16
DS26C32ATM
C76
C77
C78
C79
C80
C81
C82
C83
C84
R73
R76
TP17
TP18
TP19
TP20
APD_IN16
APD_IN17
APD_IN18
APD_IN19
APD_EXT_1_16
APD_EXT_2_16
APD_EXT_2_18
APD_EXT_1_18
APD_EXT_1_17
APD_EXT_2_17
APD_EXT_2_19
APD_EXT_1_19
GND
+5V

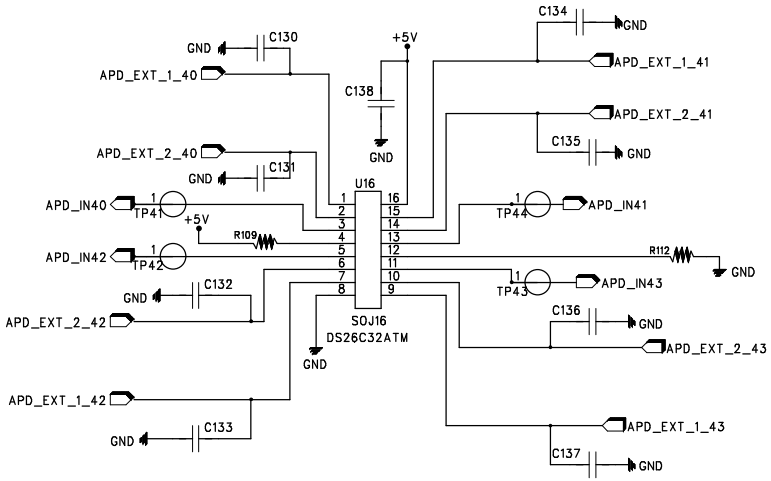

U11
SOJ16
DS26C32ATM
C85
C86
C87
C88
C89
C90
C91
C92
C93
R79
R82
TP21
TP22
TP23
TP24
APD_IN20
APD_IN21
APD_IN22
APD_IN23
APD_EXT_1_20
APD_EXT_2_20
APD_EXT_2_22
APD_EXT_1_22
APD_EXT_1_21
APD_EXT_2_21
APD_EXT_2_23
APD_EXT_1_23
GND
+5V

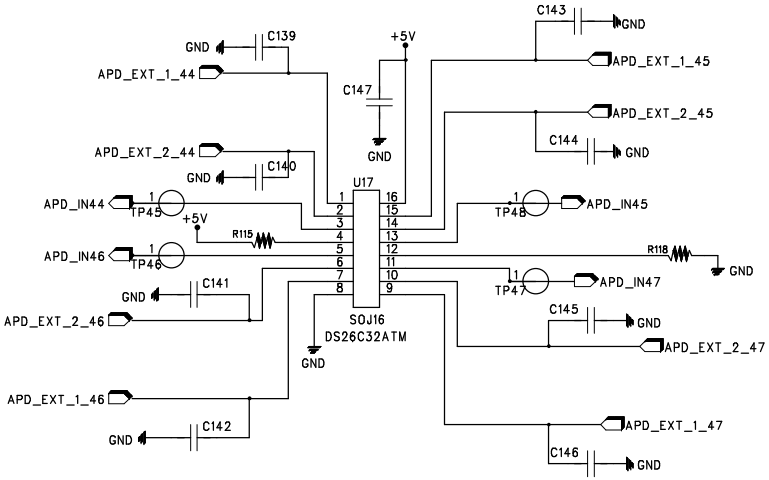

U12
SOJ16
DS26C32ATM
C94
C95
C96
C97
C98
C99
C100
C101
C102
R85
R88
TP25
TP26
TP27
TP28
APD_IN24
APD_IN25
APD_IN26
APD_IN27
APD_EXT_1_24
APD_EXT_2_24
APD_EXT_2_26
APD_EXT_1_26
APD_EXT_1_25
APD_EXT_2_25
APD_EXT_2_27
APD_EXT_1_27
GND
+5V

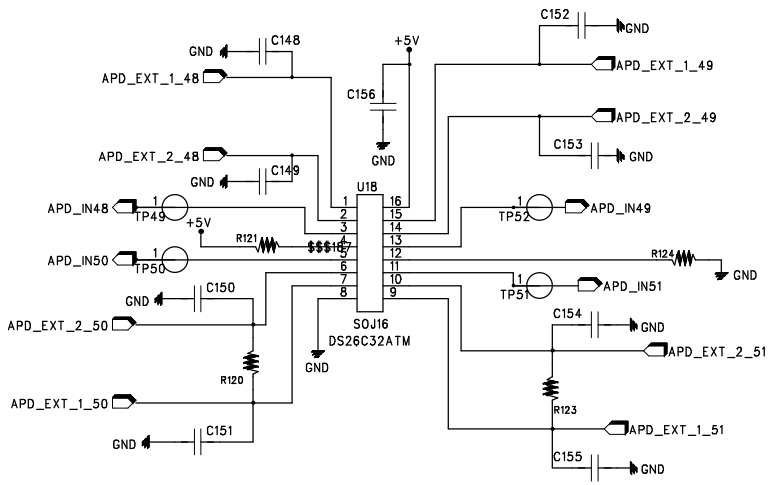

U13
SOJ16
DS26C32ATM
C103
C104
C105
C106
C107
C108
C109
C110
C111
R91
R94
TP29
TP30
TP31
TP32
APD_IN28
APD_IN29
APD_IN30
APD_IN31
APD_EXT_1_28
APD_EXT_2_28
APD_EXT_2_30
APD_EXT_1_30
APD_EXT_1_29
APD_EXT_2_29
APD_EXT_2_31
APD_EXT_1_31
GND
+5V

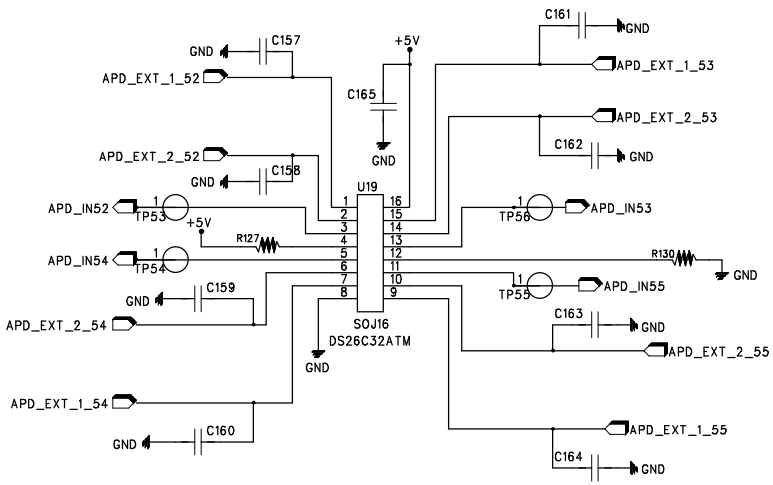

U14
SOJ16
DS26C32ATM
+5V
GND
C112
C113
C114
C115
C116
C117
C118
C119
C120
R97
R100
TP33
TP34
TP35
TP36
APD_IN32
APD_IN33
APD_IN34
APD_IN35
APD_EXT_1_32
APD_EXT_2_32
APD_EXT_2_34
APD_EXT_1_34
APD_EXT_1_33
APD_EXT_2_33
APD_EXT_2_35
APD_EXT_1_35

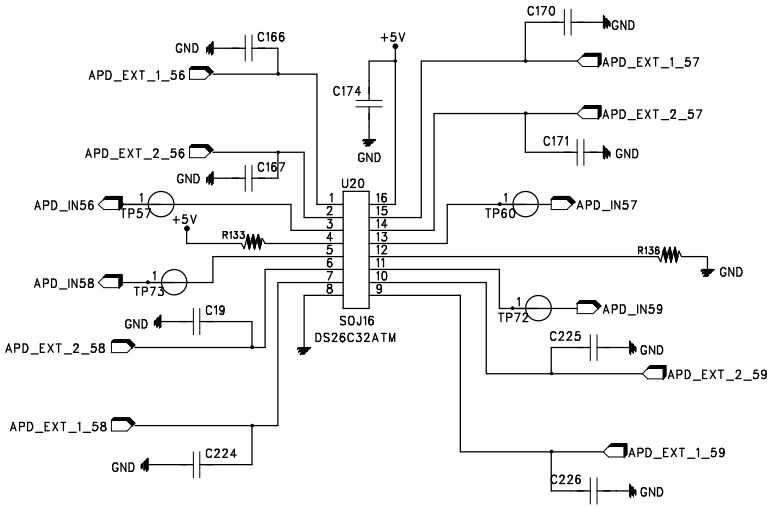

U15
SOJ16
DS26C32ATM
+5V
GND
C121
C122
C123
C124
C125
C126
C127
C128
C129
R103
R106
TP37
TP38
TP39
TP40
APD_IN36
APD_IN37
APD_IN38
APD_IN39
APD_EXT_1_36
APD_EXT_2_36
APD_EXT_2_38
APD_EXT_1_38
APD_EXT_1_37
APD_EXT_2_37
APD_EXT_2_39
APD_EXT_1_39

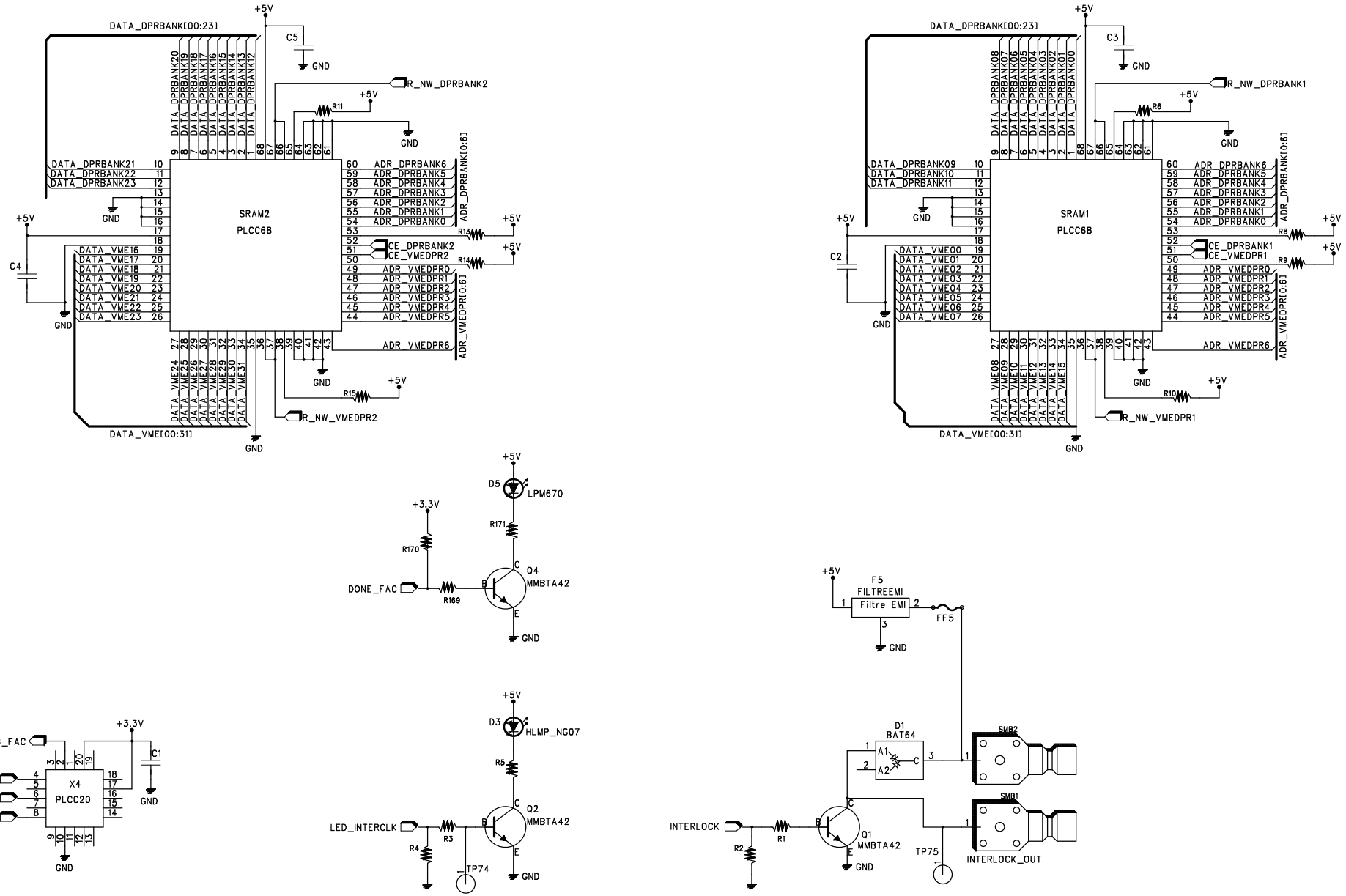

U16
SOJ16
DS26C32ATM
+5V
GND
C130
C131
C132
C133
C134
C135
C136
C137
C138
R109
R112
TP41
TP42
TP43
TP44
APD_IN40
APD_IN41
APD_IN42
APD_IN43
APD_EXT_1_40
APD_EXT_2_40
APD_EXT_2_42
APD_EXT_1_42
APD_EXT_1_41
APD_EXT_2_41
APD_EXT_2_43
APD_EXT_1_43

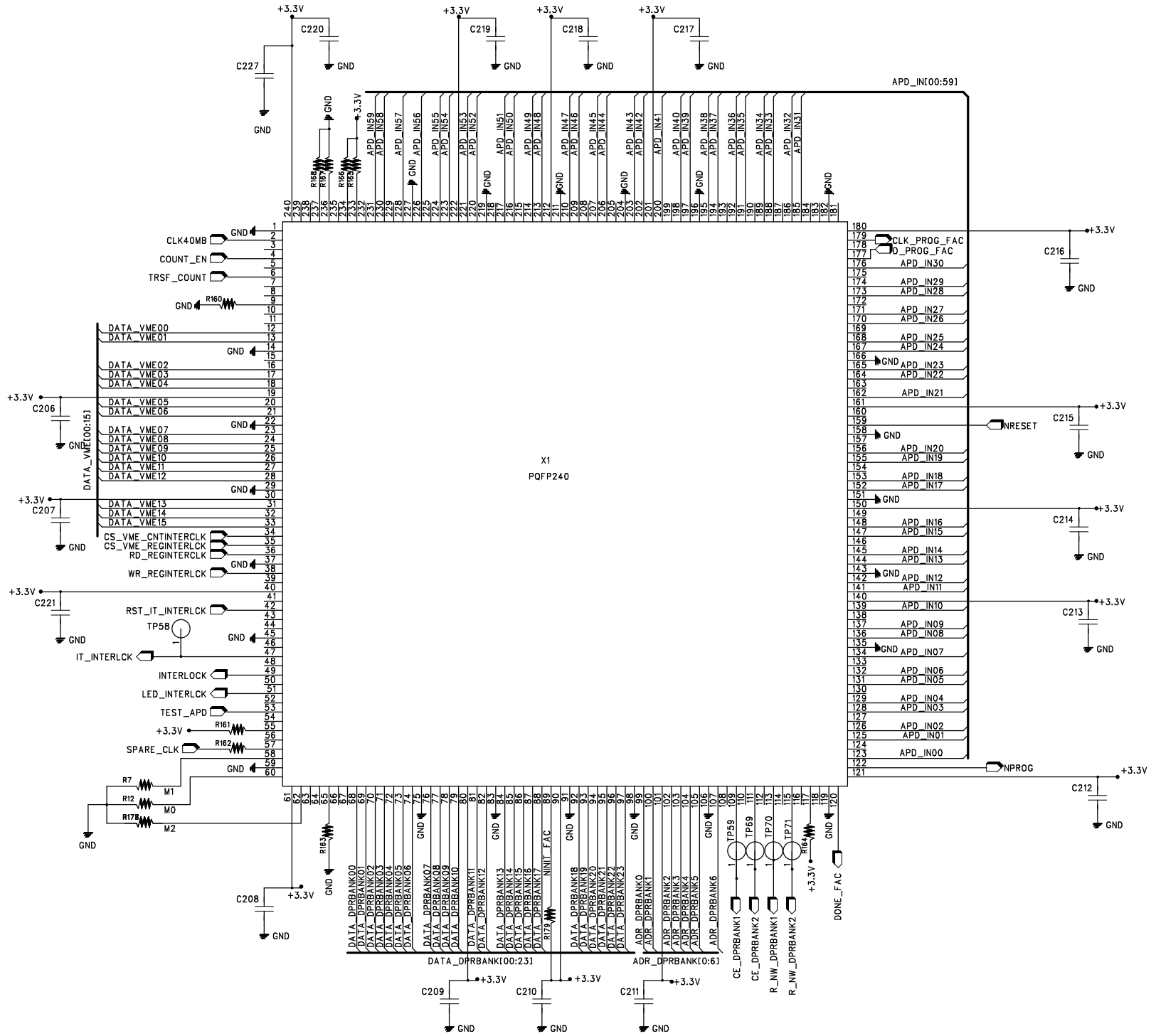

U17
SOJ16
DS26C32ATM
+5V
GND
C139
C140
C141
C142
C143
C144
C145
C146
C147
R115
R118
TP45
TP46
TP47
TP48
APD_IN44
APD_IN45
APD_IN46
APD_IN47
APD_EXT_1_44
APD_EXT_2_44
APD_EXT_2_46
APD_EXT_1_46
APD_EXT_1_45
APD_EXT_2_45
APD_EXT_2_47
APD_EXT_1_47

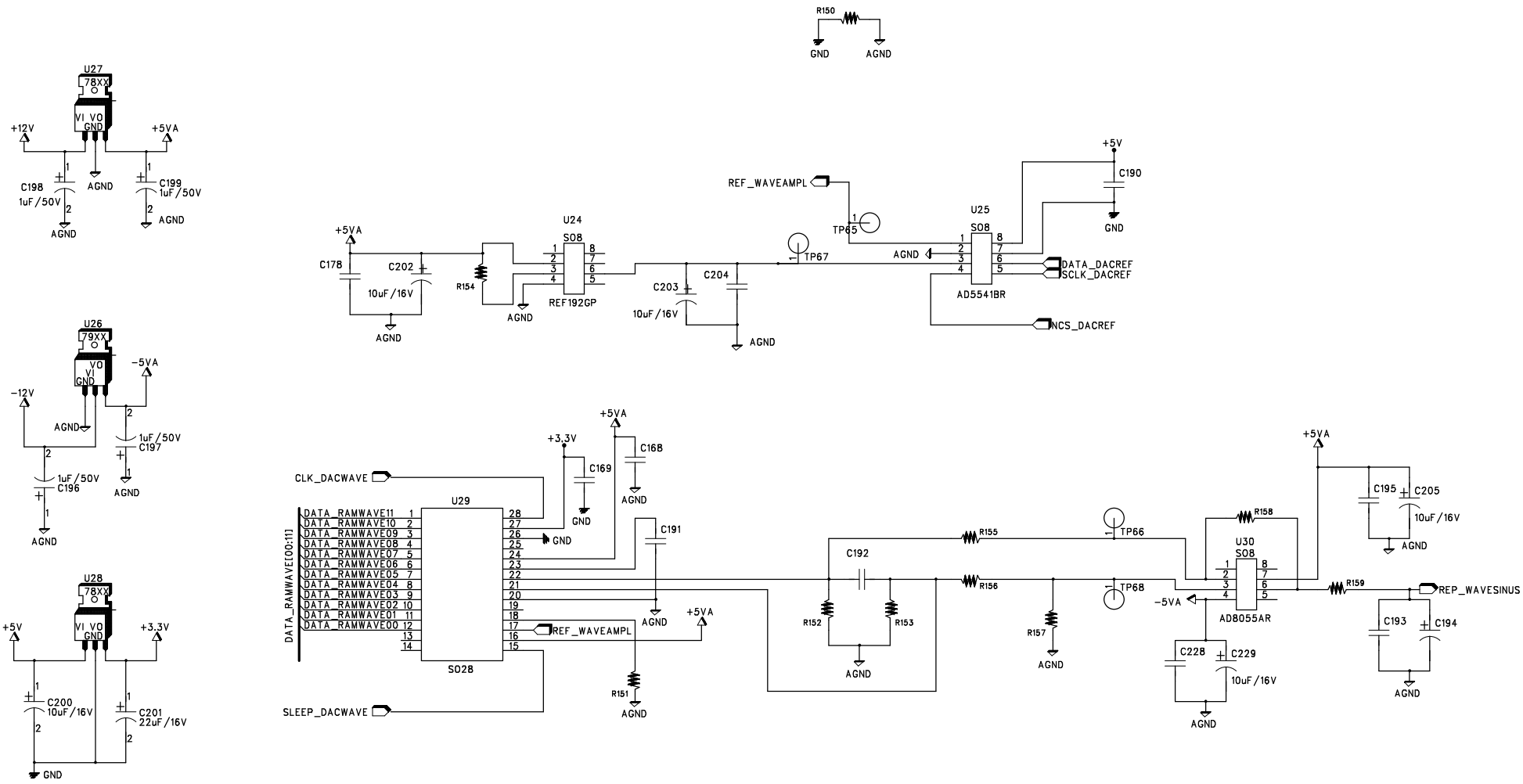

C148
GND
APD_EXT_1_48
+5V
C156
GND
C152
GND
APD_EXT_1_49
APD_EXT_2_49
C153
GND
APD_EXT_2_48
C149
GND
U18
APD_IN48
TP49
+5V
R121
APD_IN50
TP50
R124
GND
C150
GND
APD_EXT_2_50
TP52
APD_IN49
TP51
APD_IN51
C154
GND
APD_EXT_2_51
SOJ16
DS26C32ATM
GND
R120
R123
APD_EXT_1_50
APD_EXT_1_51
C151
GND
C155
GND

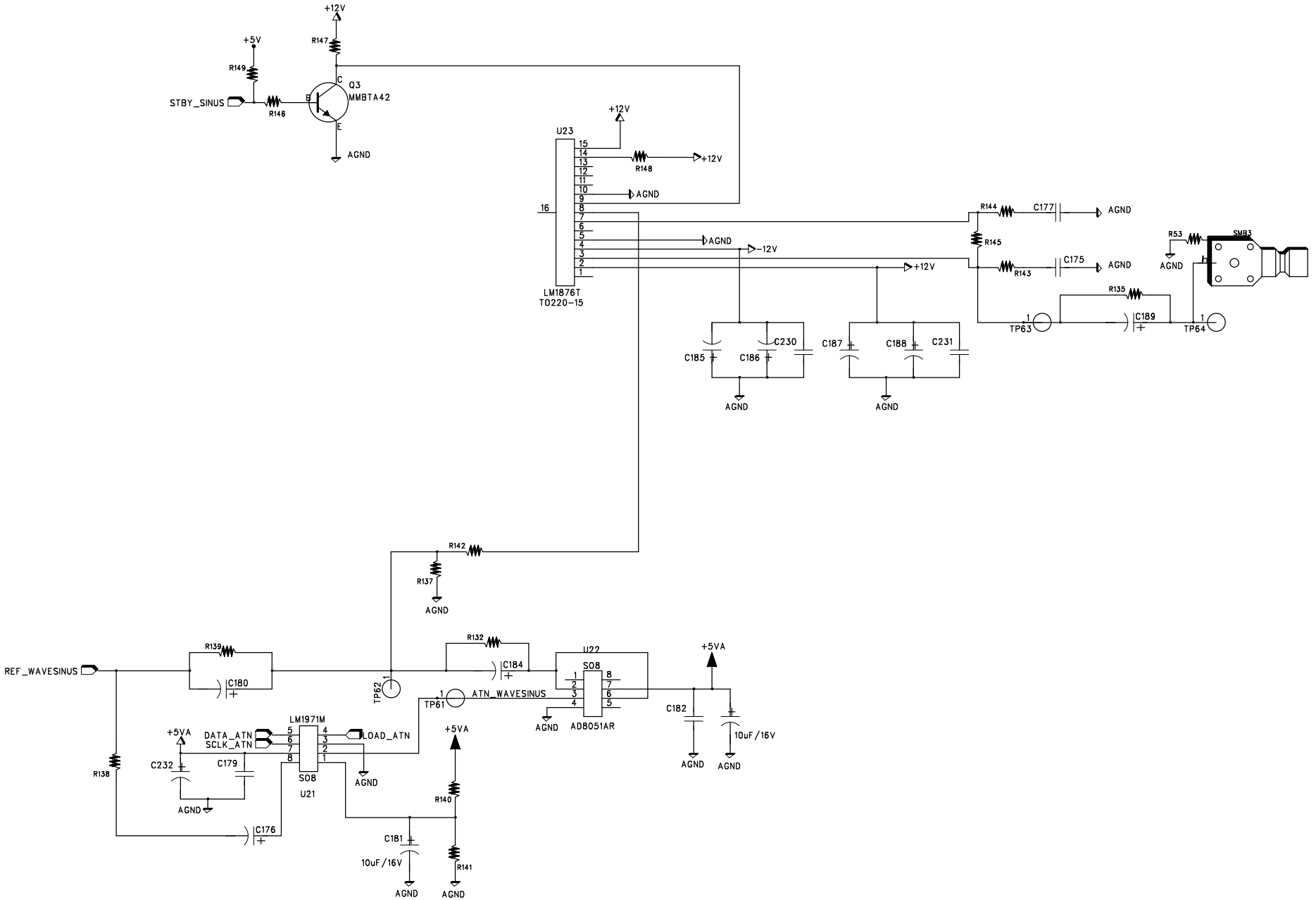

C157
GND
APD_EXT_1_52
+5V
C165
GND
C161
GND
APD_EXT_1_53
APD_EXT_2_53
C162
GND
APD_EXT_2_52
C158
GND
U19
APD_IN52
TP53
+5V
R127
APD_IN54
TP54
R130
GND
C159
GND
APD_EXT_2_54
TP56
APD_IN53
TP55
APD_IN55
C163
GND
APD_EXT_2_55
SOJ16
DS26C32ATM
GND
APD_EXT_1_54
APD_EXT_1_55
C160
GND
C164
GND

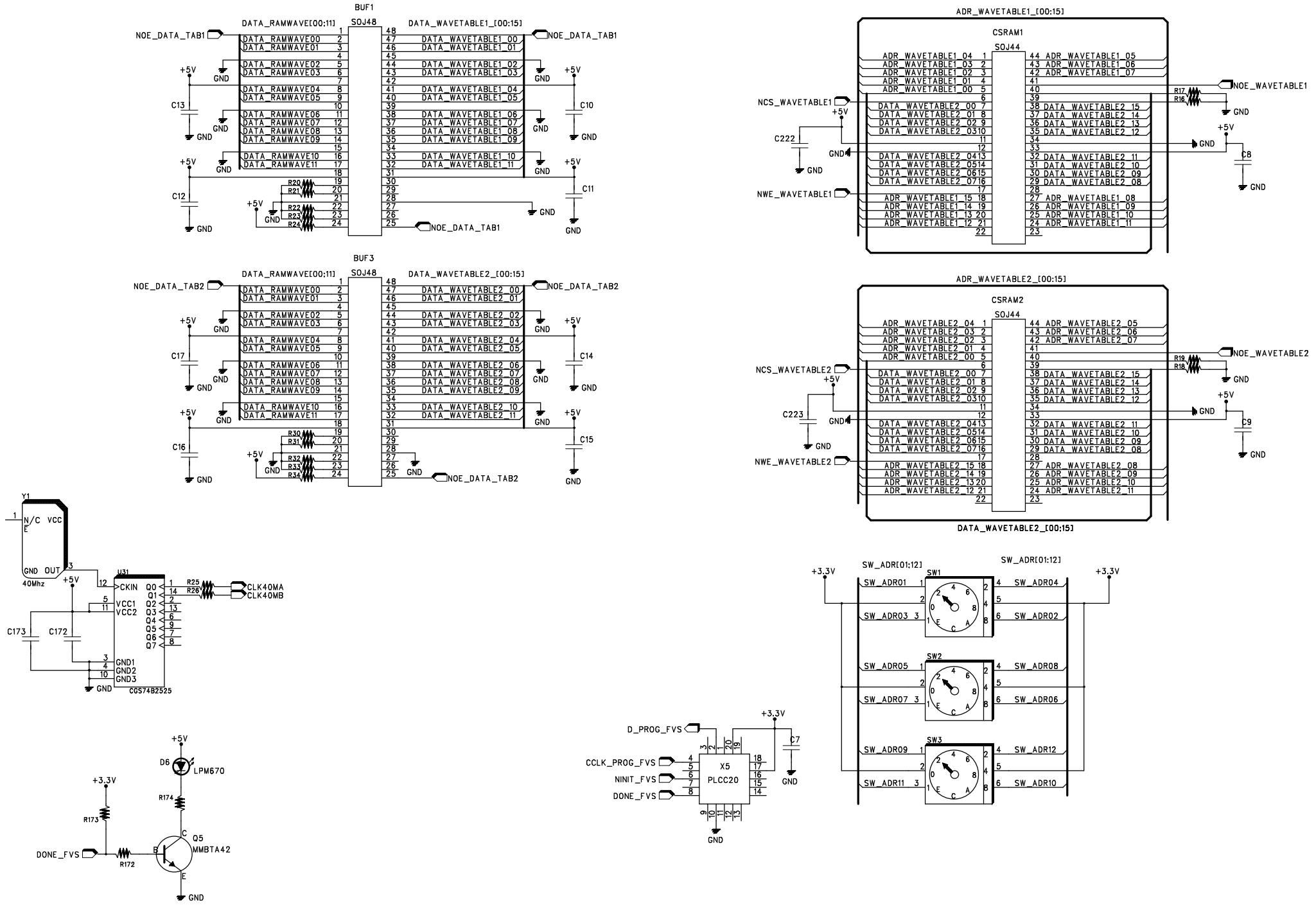

C166
GND
APD_EXT_1_56
+5V
C174
GND
C170
GND
APD_EXT_1_57
APD_EXT_2_57
C171
GND
APD_EXT_2_56
C167
GND
U20
APD_IN56
TP57
+5V
R133
TP60
APD_IN57
R136
GND
APD_IN58
TP73
C19
GND
APD_EXT_2_58
TP72
APD_IN59
C225
GND
APD_EXT_2_59
SOJ16
DS26C32ATM
APD_EXT_1_58
APD_EXT_1_59
C224
GND
C226
GND

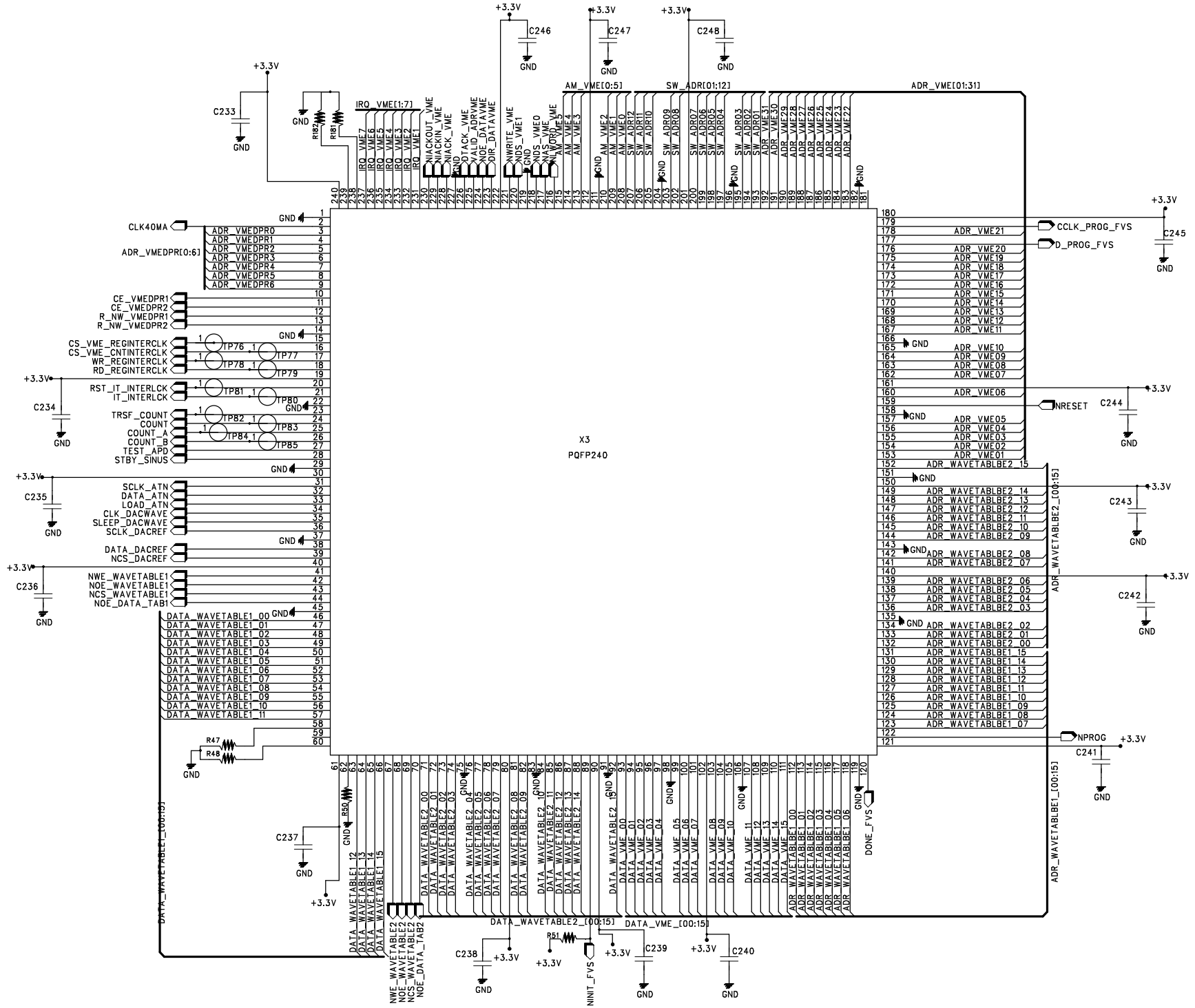

SRAM2
PLCC68
SRAM1
PLCC68
DATA_DPRBANK[00:23]
DATA_VME[00:31]
ADR_DPRBANK[0:6]
ADR_VMEDPR[0:6]
R_NW_DPRBANK2
R_NW_DPRBANK1
R_NW_VMEDPR2
R_NW_VMEDPR1
CE_DPRBANK2
CE_VMEDPR2
CE_DPRBANK1
CE_VMEDPR1
C5
C3
C4
C2
R11
R6
R13
R14
R8
R9
R15
R10
+5V
GND
D5
LPM670
R171
R170
R169
Q4
MMBTA42
DONE_FAC
+3.3V
F5
FILTREEMI
Filtre EMI
FF5
D1
BAT64
SMB2
SMB1
INTERLOCK_OUT
INTERLOCK
R1
R2
Q1
MMBTA42
TP75
D_PROG_FAC
CCLK_PROG_FAC
NINIT_FAC
DONE_FAC
X4
PLCC20
C1
D3
HLMP_NG07
R5
R3
R4
Q2
MMBTA42
LED_INTERCLK
TP74

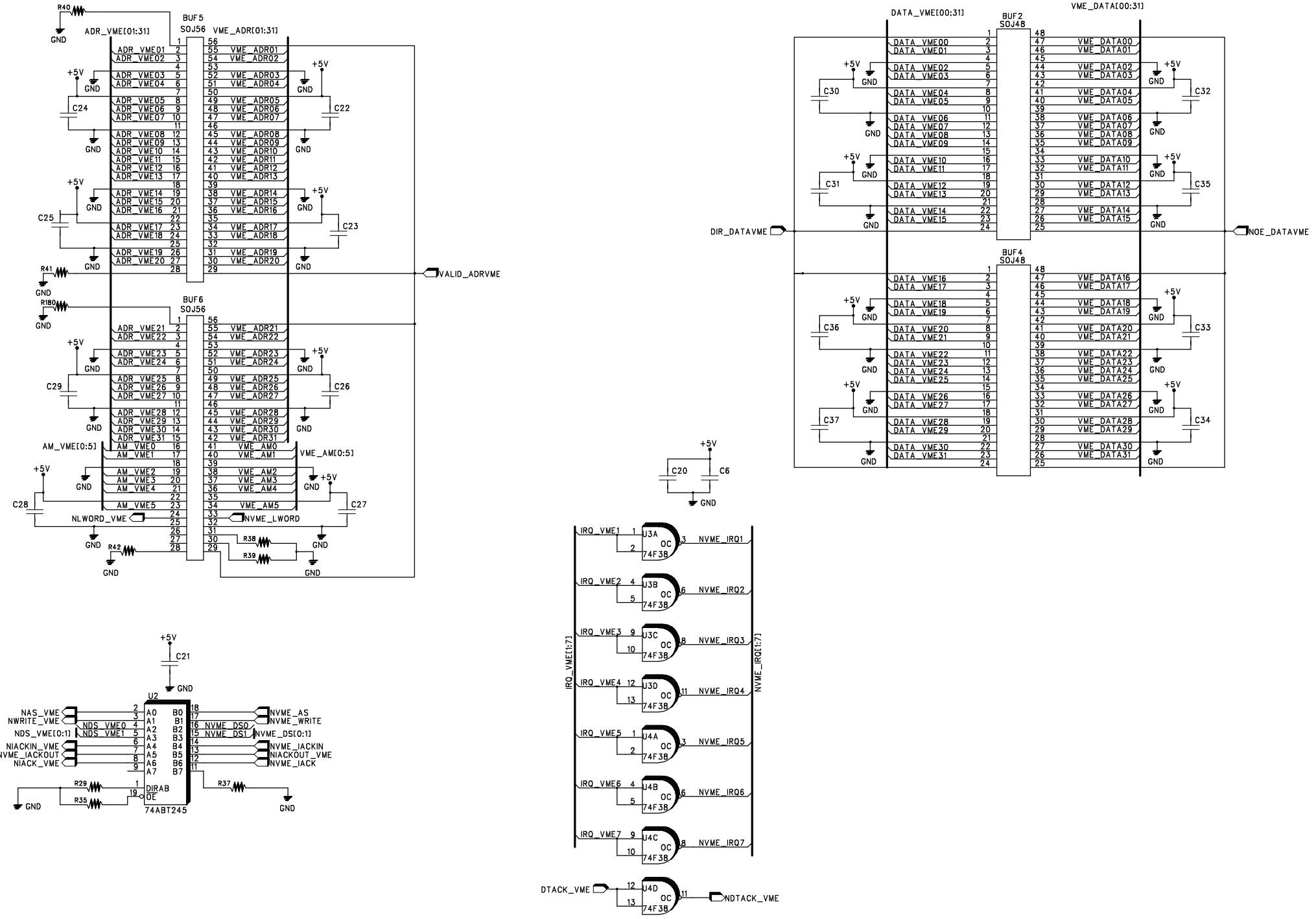

X1
PQFP240
APD_IN[00:59]
DATA_VME[00:15]
DATA_DPRBANK[00:23]
ADR_DPRBANK[0:6]
CLK40MB
COUNT_EN
TRSF_COUNT
CS_VME_CNTINTERCLK
CS_VME_REGINTERCLK
RD_REGINTERCLK
WR_REGINTERCLK
RST_IT_INTERLCK
IT_INTERLCK
INTERLOCK
LED_INTERLCK
TEST_APD
SPARE_CLK
NINIT_FAC
CLK_PROG_FAC
D_PROG_FAC
NRESET
NPROG
DONE_FAC
CE_DPRBANK1
CE_DPRBANK2
R_NW_DPRBANK1
R_NW_DPRBANK2
+3.3V
GND


U27
78XX
VI VO
GND
+12V
+5VA
C198
1uF/50V
C199
1uF/50V
AGND
U26
79XX
VO
VI
GND
-12V
-5VA
C196
1uF/50V
C197
1uF/50V
U28
78XX
+5V
+3.3V
C200
10uF/16V
C201
22uF/16V
GND
R150
GND
AGND
U24
SO8
REF192GP
+5VA
C178
C202
10uF/16V
R154
C203
10uF/16V
C204
REF_WAVEAMPL
TP65
TP67
U25
SO8
AD5541BR
+5V
C190
DATA_DACREF
SCLK_DACREF
NCS_DACREF
U29
SO28
DATA_RAMWAVE[00:11]
DATA_RAMWAVE11
DATA_RAMWAVE10
DATA_RAMWAVE09
DATA_RAMWAVE08
DATA_RAMWAVE07
DATA_RAMWAVE06
DATA_RAMWAVE05
DATA_RAMWAVE04
DATA_RAMWAVE03
DATA_RAMWAVE02
DATA_RAMWAVE01
DATA_RAMWAVE00
CLK_DACWAVE
SLEEP_DACWAVE
+3.3V
C169
C168
C191
R151
C192
R152
R153
R155
R156
R157
TP66
TP68
U30
SO8
AD8055AR
R158
R159
C228
C229
10uF/16V
C195
C205
10uF/16V
C193
C194
REP_WAVESINUS


+12V
+5V
R147
R149
Q3
MMBTA42
STBY_SINUS
R146
AGND
U23
R148
+12V
AGND
16
-12V
LM1876T
TO220-15
R144
C177
R145
R143
C175
R53
SMB3
R135
TP63
C189
TP64
C185
C186
C230
C187
C188
C231
R142
R137
R139
C180
R132
C184
U22
SO8
AD8051AR
+5VA
REF_WAVESINUS
TP62
TP61
ATN_WAVESINUS
C182
10uF/16V
LM1971M
DATA_ATN
SCLK_ATN
LOAD_ATN
R138
C232
C179
U21
R140
C176
C181
R141


BUF1
SOJ48
DATA_RAMWAVE[00:11]
DATA_WAVETABLE1_[00:15]
NOE_DATA_TAB1
DATA_RAMWAVE00
DATA_RAMWAVE01
DATA_RAMWAVE02
DATA_RAMWAVE03
DATA_RAMWAVE04
DATA_RAMWAVE05
DATA_RAMWAVE06
DATA_RAMWAVE07
DATA_RAMWAVE08
DATA_RAMWAVE09
DATA_RAMWAVE10
DATA_RAMWAVE11
DATA_WAVETABLE1_00
DATA_WAVETABLE1_01
DATA_WAVETABLE1_02
DATA_WAVETABLE1_03
DATA_WAVETABLE1_04
DATA_WAVETABLE1_05
DATA_WAVETABLE1_06
DATA_WAVETABLE1_07
DATA_WAVETABLE1_08
DATA_WAVETABLE1_09
DATA_WAVETABLE1_10
DATA_WAVETABLE1_11
+5V
GND
C13
C10
C12
C11
R20
R21
R22
R23
R24
BUF3
SOJ48
DATA_RAMWAVE[00:11]
DATA_WAVETABLE2_[00:15]
NOE_DATA_TAB2
DATA_WAVETABLE2_00
DATA_WAVETABLE2_01
DATA_WAVETABLE2_02
DATA_WAVETABLE2_03
DATA_WAVETABLE2_04
DATA_WAVETABLE2_05
DATA_WAVETABLE2_06
DATA_WAVETABLE2_07
DATA_WAVETABLE2_08
DATA_WAVETABLE2_09
DATA_WAVETABLE2_10
DATA_WAVETABLE2_11
C17
C14
C16
C15
R30
R31
R32
R33
R34
ADR_WAVETABLE1_[00:15]
CSRAM1
SOJ44
ADR_WAVETABLE1_04
ADR_WAVETABLE1_03
ADR_WAVETABLE1_02
ADR_WAVETABLE1_01
ADR_WAVETABLE1_00
ADR_WAVETABLE1_05
ADR_WAVETABLE1_06
ADR_WAVETABLE1_07
ADR_WAVETABLE1_08
ADR_WAVETABLE1_09
ADR_WAVETABLE1_10
ADR_WAVETABLE1_11
DATA_WAVETABLE2_00
DATA_WAVETABLE2_01
DATA_WAVETABLE2_02
DATA_WAVETABLE2_03
DATA_WAVETABLE2_04
DATA_WAVETABLE2_05
DATA_WAVETABLE2_06
DATA_WAVETABLE2_07
DATA_WAVETABLE2_08
DATA_WAVETABLE2_09
DATA_WAVETABLE2_10
DATA_WAVETABLE2_11
NCS_WAVETABLE1
NWE_WAVETABLE1
NOE_WAVETABLE1
R17
R16
C222
C8
ADR_WAVETABLE2_[00:15]
CSRAM2
SOJ44
ADR_WAVETABLE2_04
ADR_WAVETABLE2_03
ADR_WAVETABLE2_02
ADR_WAVETABLE2_01
ADR_WAVETABLE2_00
ADR_WAVETABLE2_05
ADR_WAVETABLE2_06
ADR_WAVETABLE2_07
ADR_WAVETABLE2_08
ADR_WAVETABLE2_09
ADR_WAVETABLE2_10
ADR_WAVETABLE2_11
NCS_WAVETABLE2
NWE_WAVETABLE2
NOE_WAVETABLE2
R19
R18
C223
C9
DATA_WAVETABLE2_[00:15]
Y1
40Mhz
N/C
VCC
GND
OUT
U31
CKIN
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
VCC1
VCC2
GND1
GND2
GND3
CGS74B2525
R25
R26
CLK40MA
CLK40MB
C173
C172
D6
LPM670
R174
R173
R172
Q5
MMBTA42
DONE_FVS
D_PROG_FVS
CCLK_PROG_FVS
NINIT_FVS
DONE_FVS
X5
PLCC20
C7
+3.3V
SW_ADR[01:12]
SW1
SW2
SW3
SW_ADR01
SW_ADR03
SW_ADR04
SW_ADR02
SW_ADR05
SW_ADR07
SW_ADR08
SW_ADR06
SW_ADR09
SW_ADR11
SW_ADR12
SW_ADR10

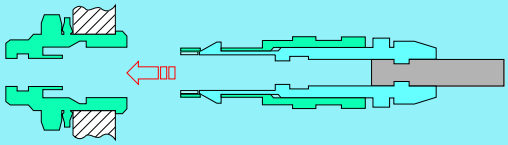

X3
PQFP240
+3.3V
GND
C233
C234
C235
C236
C237
C238
C239
C240
C241
C242
C243
C244
C245
C246
C247
C248
R47
R48
R50
R51
R181
R182
TP76
TP77
TP78
TP79
TP80
TP81
TP82
TP83
TP84
TP85
IRQ_VME[1:7]
AM_VME[0:5]
SW_ADR[01:12]
ADR_VME[01:31]
CLK40MA
ADR_VMEDPR[0:6]
CE_VMEDPR1
CE_VMEDPR2
R_NW_VMEDPR1
R_NW_VMEDPR2
CS_VME_REGINTERCLK
CS_VME_CNTINTERCLK
WR_REGINTERCLK
RD_REGINTERCLK
RST_IT_INTERLCK
IT_INTERLCK
TRSF_COUNT
COUNT
COUNT_A
COUNT_B
TEST_APD
STBY_SINUS
SCLK_ATN
DATA_ATN
LOAD_ATN
CLK_DACWAVE
SLEEP_DACWAVE
SCLK_DACREF
DATA_DACREF
NCS_DACREF
NWE_WAVETABLE1
NOE_WAVETABLE1
NCS_WAVETABLE1
NOE_DATA_TAB1
DATA_WAVETABLE1_[00:15]
DATA_WAVETABLE2_[00:15]
DATA_VME_[00:15]
ADR_WAVETABLBE2_[00:15]
ADR_WAVETABLBE1_[00:15]
CCLK_PROG_FVS
D_PROG_FVS
NRESET
NPROG
DONE_FVS
NINIT_FVS
NWE_WAVETABLE2
NOE_WAVETABLE2
NCS_WAVETABLE2
NOE_DATA_TAB2

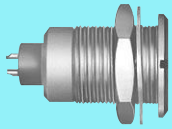

BUF5
SOJ56
BUF6
SOJ56
ADR_VME[01:31]
VME_ADR[01:31]
VALID_ADRVME
AM_VME[0:5]
VME_AM[0:5]
NLWORD_VME
NVME_LWORD
R40
R41
R180
R42
R38
R39
C24
C22
C25
C23
C29
C26
C28
C27
BUF2
SOJ48
BUF4
SOJ48
DATA_VME[00:31]
VME_DATA[00:31]
DIR_DATAVME
NOE_DATAVME
C30
C32
C31
C35
C36
C33
C37
C34
C20
C6
U2
74ABT245
NAS_VME
NWRITE_VME
NDS_VME[0:1]
NIACKIN_VME
NVME_IACKOUT
NIACK_VME
NVME_AS
NVME_WRITE
NVME_DS[0:1]
NVME_IACKIN
NIACKOUT_VME
NVME_IACK
R29
R35
R37
C21
IRQ_VME[1:7]
NVME_IRQ[1:7]
U3A
U3B
U3C
U3D
U4A
U4B
U4C
U4D
74F38
DTACK_VME
NDTACK_VME
+5V
GND

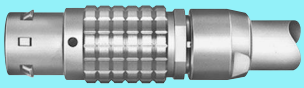
13. ANNEXES 2 LEMO CONNECTOR

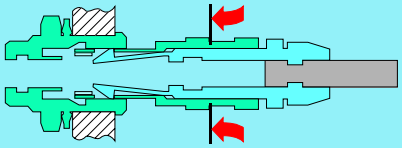
LEMO's Push-Pull Self-Latching Connection System

This self-latching system is renowned worldwide for its easy and quick mating and unmating features. It provides absolute security against vibration, shock or pull on the cable, and facilitates operation in a very limited space.

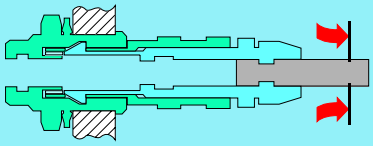




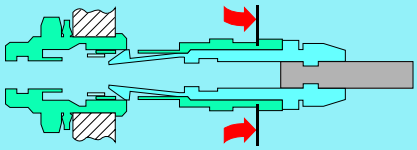




The LEMO self-latching system allows the connector to be mated by simply pushing the plug axially into socket.



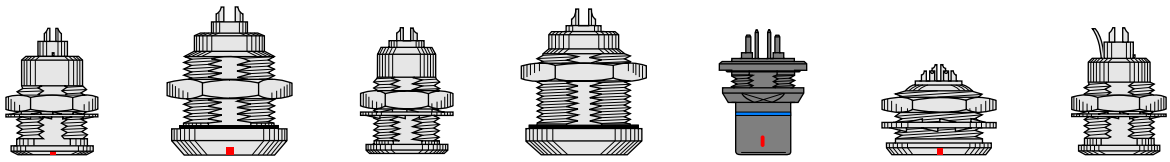
Once firmly latched, connection cannot be broken by pulling on the cable or any other component part other than the outer release sleeve.

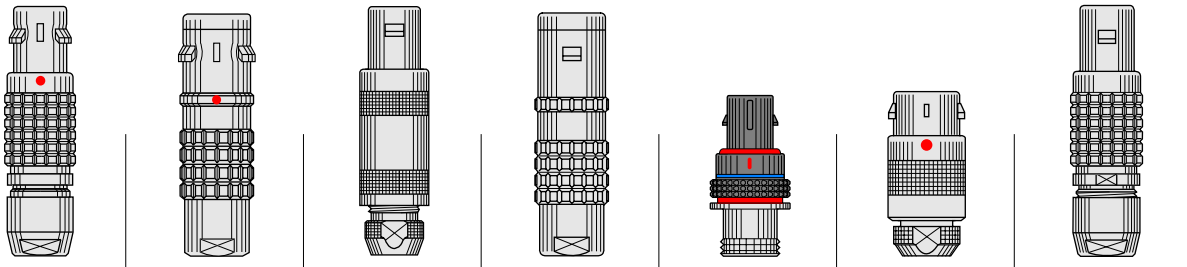


When required, the connector is disengaged by a single axial pull on the outer release sleeve. This first disengages the latches and then withdraws the plug from the socket.

Unipole and Multipole Connectors Production Programme

The production programme is divided into 7 families of connectors. Their main characteristics and features are shown below.



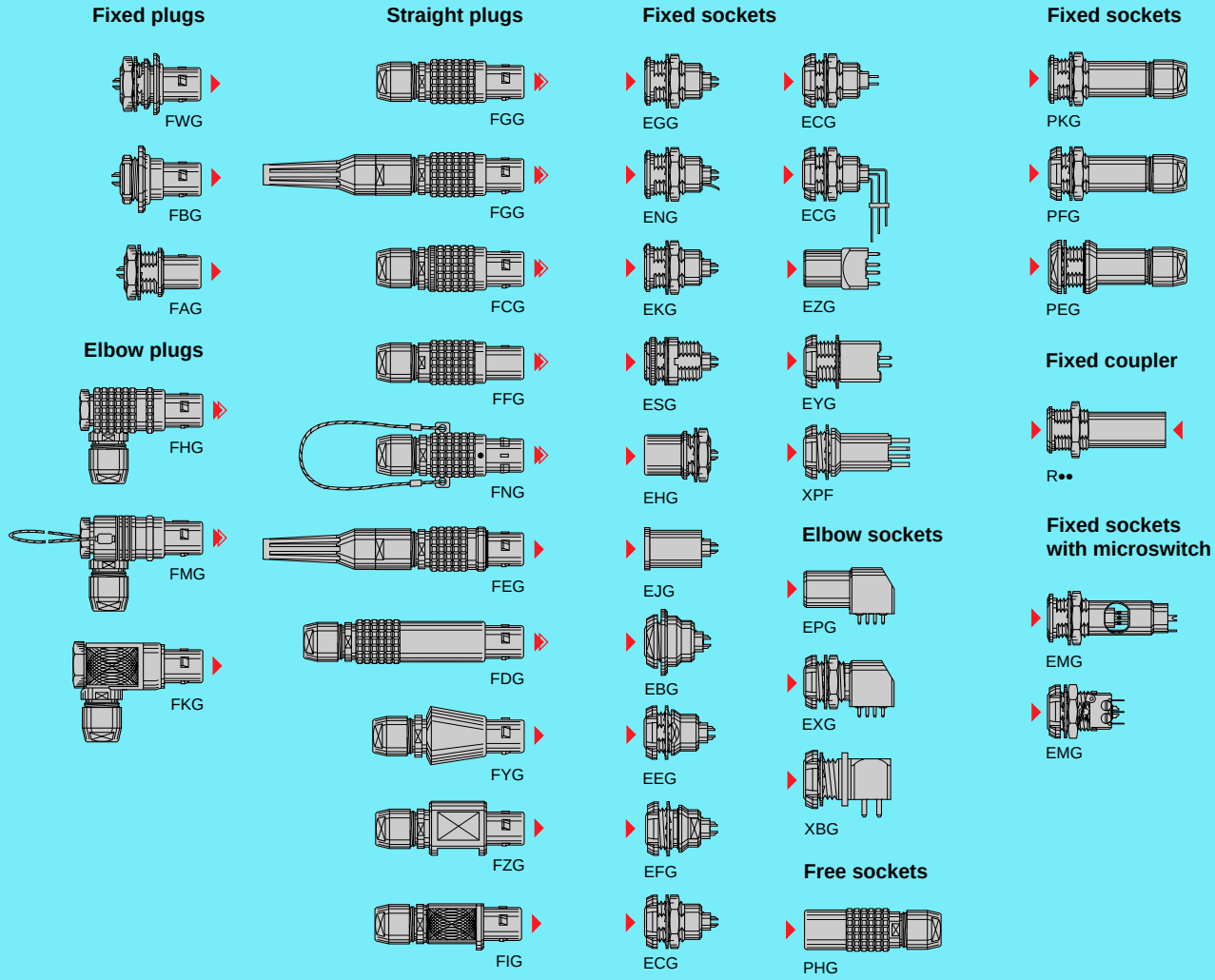


Series	00 multipole 0B to 5B	0K to 5K	00 unipole 0S to 6S	0E to 6E	0F to 5F	2C/2G	1D
Latching	Push-Pull						
Shell	Metal or plastic	Metal	Metal or plastic	Metal	Metal		
Feature	Keyed	Keyed watertight	Hermaphroditic insert	Watertight hermaphroditic	Light compact	Shortened version	4 concentric contacts
Insulator type	Multipole		Multipole or unipole		Multipole		Quadrax
Contact type	Solder, crimp or print		Solder or print		Crimp or print	Solder or print	Solder
Page	13 to 40	41 to 54	67 to 90	91 to 102	125 to 140	141 to 156	157 to 164

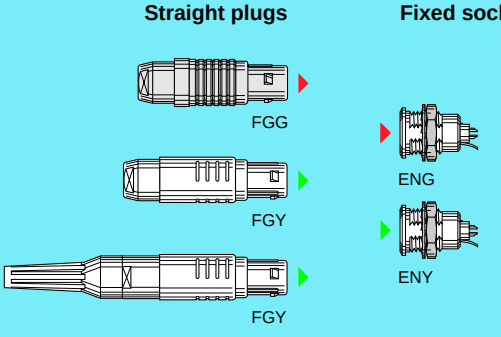
B Series

B series connectors provide the following main features:
– security of the Push-Pull self-latching system
– multipole types 2 to 64 contacts
– solder, crimp or print contacts (straight or elbow)
– keying system («G» key standard) for connector alignment
– multiple key options to avoid cross mating of similar connectors
– high packing density for space savings
– 360° screening for full EMC shielding.

Interconnections



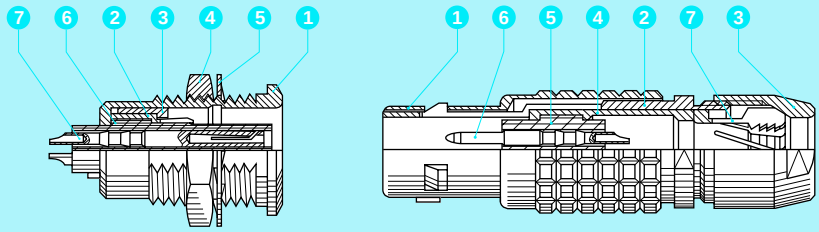
Plastic housing models



Part Section Showing Internal Components

Fixed socket

1. outer shell
2. earthing crown
3. retaining ring
4. hexagonal nut
5. locking washer
6. insulator
7. female contact



Straight plug

1. outer shell
2. latch sleeve
3. collet nut
4. split insert carrier
5. insulator
6. male contact
7. collet

Technical Characteristics

Mechanical and Climatical

Characteristics	Value	Standard
Endurance	> 5000 cycles	IEC 60512-5 test 9a
Humidity	up 95% to 60° C	
Temperature range[1)]	- 55° C, +250° C	
Resistance to vibration	10-2000 Hz, 15 g	IEC 60512-4 test 6d
Shock resistance	100 g, 6 ms	IEC 60512-4 test 6c
Salt spray corrosion test	> 144h	IEC 60512-6 test 11f
Protection index (mated)	IP50	IEC 60529
Climatical category[1)]	55/175/21	IEC 60068-1

Electrical

Characteristics		Value	Standard
Shielding efficiency	at 10 MHz	> 75 dB	IEC 60169-1-3
	at 1 GHz	> 40 dB	IEC 60169-1-3

Note:
the various tests have been carried out with FGG and EGG connector pairs, with chrome-plated brass shell and PEEK insulator.
Detailed electrical characteristics, as well as materials and treatment are presented in the chapter Technical Characteristics on page 197.
[1)] for watertight or vacuumtight models see page 37.

Available Models (series and types)

Model	Multipole						
	00	0B	1B	2B	3B	4B	5B
CFF		●	●				
CRG		●	●				
EBG							●
ECG	●	●	●	●	●	●	●
ECG [2)]		●	●	●	●		
EEG	●	●	●	●	●		●
EFG		●					
EGG	●	●	●	●	●	●	●
EHG	●	●	●	●	●		●
EJG		●	●	●			
EKG				●	●	●	●
EMG		●	●	●			
ENG		●	●	●	●	●	
ENG [3)]			●		●	●	
ENY [4)]				●	●		
EPG	●	●	●				
ESG	●		●				
EXG		●	●				
EYG		●	●				
EZG	●	●	●	●			

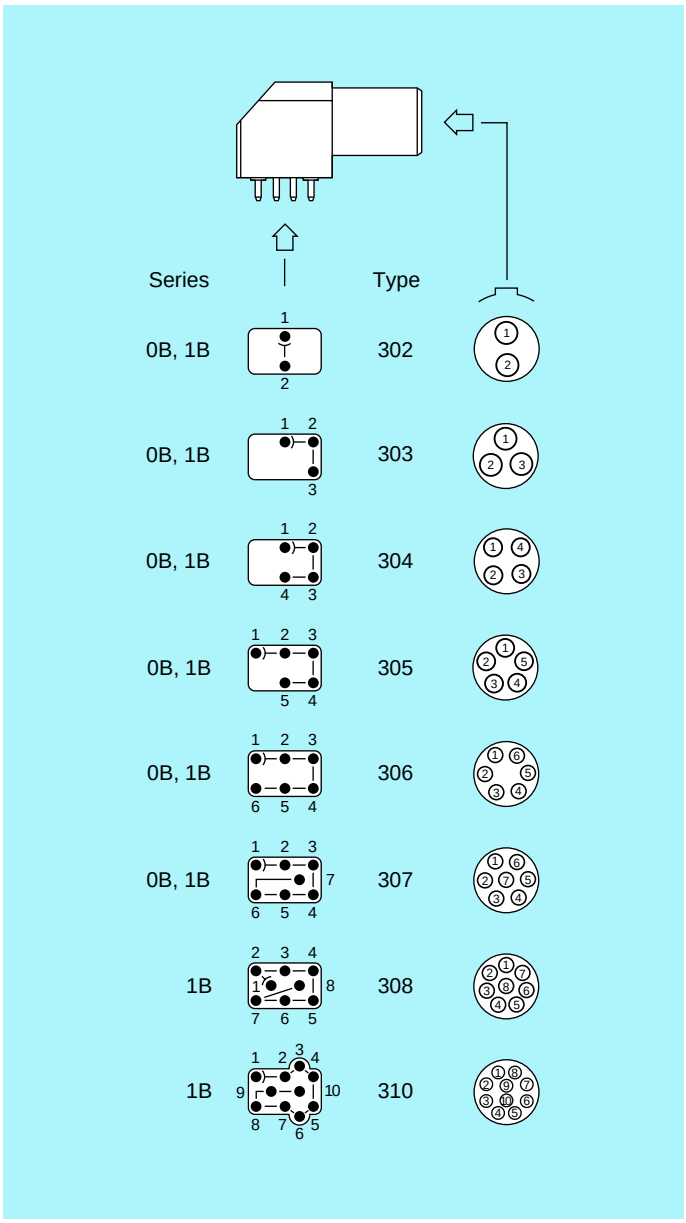
Model	Multipole						
	00	0B	1B	2B	3B	4B	5B
FAG	●	●	●	●	●	●	●
FBG							●
FCG			●			●	●
FDG			●	●			
FEG			●	●	●		
FFG		●	●	●	●	●	
FGG	●	●	●	●	●	●	●
FGG [5)]	●	●	●	●	●	●	
FGG [3)]			●		●	●	
FGY [4) 6)]				●	●		
FGY [4) 5) 6)]				●	●		
FHG	●	●	●	●	●	●	●
FIG				●	●	●	●
FKG					●	●	
FMG		●					
FNG		●	●	●	●	●	●
FTG [1)]		●					
FVB	●						
FVG	●						
FWG			●	●			

Model	Multipole						
	00	0B	1B	2B	3B	4B	5B
FYG		●					
FZG				●	●	●	●
HCG		●	●	●			
HEG				●			
HGG	●	●	●	●	●	●	●
HHG		●	●	●	●		
HMG		●	●		●		
HNG		●					
PEG					●	●	
PFG	●	●	●	●	●	●	●
PHG	●	●	●	●	●	●	●
PHG [5)]	●	●	●	●	●	●	
PKG	●	●	●	●	●	●	●
PNG			●	●	●	●	●
R●●		●	●	●	●	●	
S●●		●	●	●	●	●	●
XBG	●						
XRB	●						
XPF		●					
YHG		●	●	●	●		

Note:
CFF, CRG, EMG, EPG, EXG and FTG models are not available in all types. Please consult pages corresponding to the models.
[1)] only available with «G» key
[2)] with elbow (90°) print contact
[3)] with PEEK outer shell
[4)] only available with «Y» key
[5)] with nut for fitting a bend relief
[6)] with PSU or PPSU outer shell
● = available models by series and types

Technical Characteristics

Types



Elbow (90°) sockets for printed circuit

These socket models are fixed onto the printed circuit either by soldering the four pins, or with 4 screws (M1.6) replacing the pins.
EXG sockets are 2 nut fixing and are recommended in cases where a flexible printed circuit is used.

Materials and Treatment

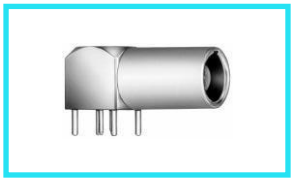
Component	Material	Surface treat. (µm)		
		Cu	Ni	Au
Housing	PPS [1]	–		
	Brass	0.5	3	–
Metallic parts	Brass	0.5	3	–
Earthing crown	Bronze	0.5	3	–
Insulator	PEEK	–		
Female contact	Bronze	0.5	3	1.5

Note: [1] not used for all sizes.
The surface treatment standards are as follows:
– Nickel: FS QQ-N-290A. – Gold: ISO 4523

Electrical

Model	Series	Types	Test voltage (kV rms)[1] Contact-contact	Test voltage (kV rms)[1] Contact-shell	Rated current (A)
EPG-XBG	00	302-303-304	1.00	1.00	2.0
EPG-EXG	0B	302	1.45	1.20	4.5
EPG-EXG	0B	303	1.70	1.60	4.5
EPG-EXG	0B	304	1.30	1.10	4.5
EPG-EXG	0B	305	1.25	1.20	4.5
EPG-EXG	0B	306	1.25	1.20	2.5
EPG-EXG	0B	307	1.00	1.00	2.0
EPG-EXG	1B	302	1.70	1.45	4.5
EPG-EXG	1B	303	1.60	1.85	4.5
EPG-EXG	1B	304	1.70	1.80	4.5
EPG-EXG	1B	305	1.30	1.55	4.5
EPG-EXG	1B	306	1.35	1.45	4.5
EPG-EXG	1B	307	1.45	1.45	2.0
EPG-EXG	1B	308	1.30	1.30	2.0
EPG-EXG	1B	310	1.00	1.00	1.5
EPG	1B	314	1.00	1.30	1.0

Note: [1] see calculation method, caution and suggested standard on page 204.

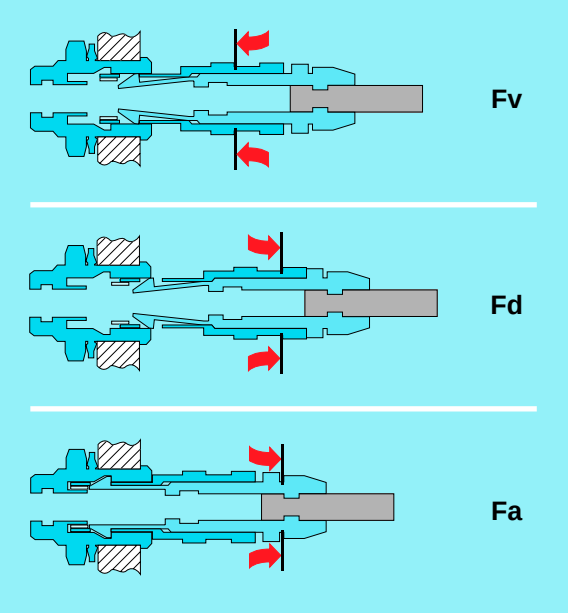


EPG Elbow (90°) socket for printed circuit, key (G) or keys (A, B)

Reference	Dimensions (mm)						
	A	D	H	I	K	L	N
EPG.00.302.NLN	6.8	11	3.5	7	7	17.5	7
EPG.00.303.NLN							
EPG.00.304.NLN							

PCB drilling pattern: **P18**

Mechanical latching characteristics



F_v: average latching force.

F_d: average unmating force with axial pull on the outer shell.

F_a: average pull force with axial pull on the collet nut

Standard series

Force (N)	Series									
	00	0S	1D	1S	2C	2S	3S	4S	5S	6S
Fv	9	14	14	15	12	17	20	40	60	70
Fd	7	9	11	10	12	11	14	25	40	55
Fa	120	140	300	250	400	350	500	650	750	900

Watertight series

Keyed series

Force (N)	Series							Series							
	0E	1E	2E	3E	4E	5E	6E	00	0B	1B	2B	2G	3B	4B	5B
Fv	14	16	20	32	65	85	100	9	10	14	15	12	17	39	48
Fd	9	10	13	25	40	60	75	7	8	11	12	12	14	38	38
Fa	250	300	400	550	700	800	900	120	250	300	400	400	550	700	800

Keyed watertight series

Force (N)	Series						Series					
	0K	1K	2K	3K	4K	5K	0F	1F	2F	3F	4F	5F
Fv	14	16	20	32	65	85	6	6	8	9	14	21
Fd	9	10	13	25	40	60	8	8	9	11	16	24
Fa	250	300	400	550	700	800	150	150	150	150	150	150

Notes: forces were measured on outer shells **not fitted with contacts**.
Mechanical endurance: 5000 cycles.
Mechanical endurance represents the number of cycles after which the latching system is still effective (1 cycle = 1 latching/unlatching at 300 cycles per hour). The values were measured according to the standard IEC 60512-7 test 13a.

1N = 0.102 kg.

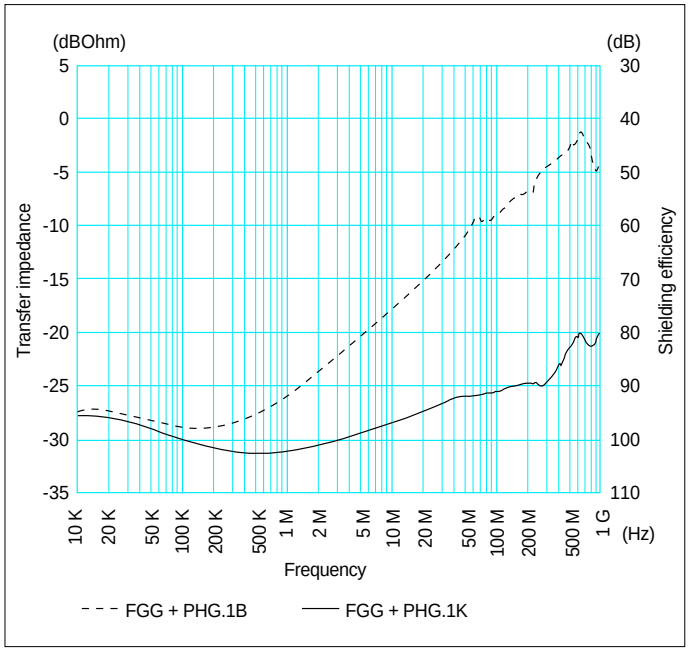
Electromagnetic compatibility (EMC) and shielding efficiency

The electromagnetic compatibility of a device can only be ensured by meeting a number of basic rules with the design of the device and by carefully selecting components, cables and connectors.

Electrical and electronic devices are to be designed to ensure the following:

a) reduce the emission of generated electromagnetic disturbance to a level where radios and telecommunication and other devices can properly function;
b) electromagnetic immunity against electromagnetic disturbance so that they can properly function.

When selecting a connector, screen or shielding efficiency and low resistance to electric continuity between the cable and the connector should be considered.
The design of LEMO connectors with metal shell and earthing crown guarantee optimum shielding efficiency in all applications where electromagnetic compatibility (EMC) is critical.
The performance of a connector is measured through shielding efficiency, a value that represents the ratio between the electromagnetic field on the outside and the inside of the shell. Our measurements are carried out according to the IEC 60169-1-3 standard.



The performance of S and B series connectors is comparable to the results of measurements carried out on a pair of FGG + PHG.1B connectors.

The performance of E and K series connectors is comparable to the results of measurements carried out on a pair of FGG + PHG.1K connectors.

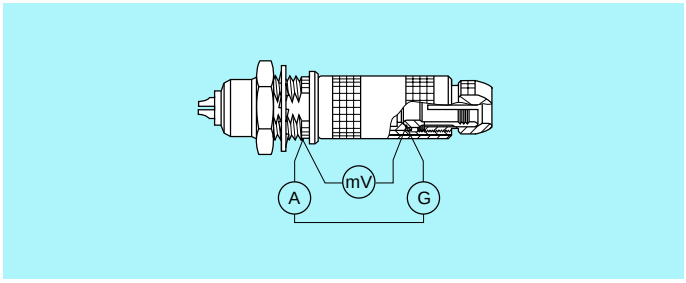
Shell electrical continuity:
(measured according to IEC 60512-2 test 2f)

Test current: 1A
A = Ammeter
mV = Millivoltmeter
G = Generator

R_1 Values with earthing crown and latch sleeve or inner-sleeve nickel-plated.

R_2 Values with gold-plated earthing crown and nickel-plated latch sleeve or inner sleeve.

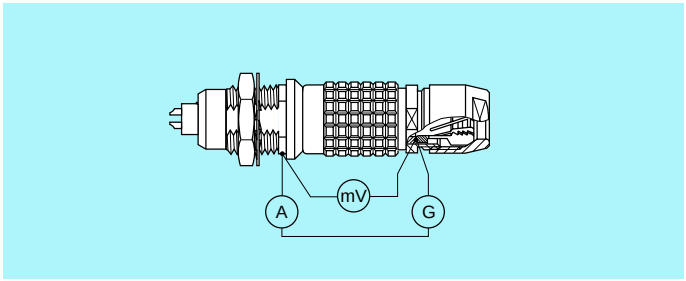
Standard series



Series	R_1 (mΩ)	R_2 (mΩ)
00	3.5	2.8
0S	2.8	1.6
1D	2.5	1.1
1S	2.2	1.5
2C	–	–

Series	R_1 (mΩ)	R_2 (mΩ)
2S	1.8	1.2
3S	1.6	1.2
4S	1.4	1.0
5S	1.4	1.0
6S	1.0	0.5

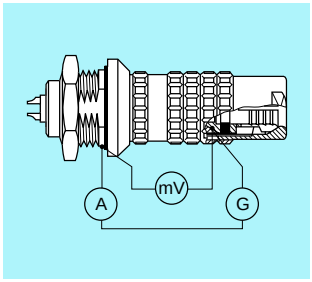
Keyed series



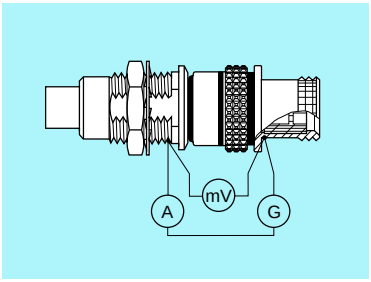
Series	R_1 (mΩ)	R_2 (mΩ)
00	3.5	2.8
0B	3.5	1.3
1B	2.5	1.1
2B	2.2	0.9

Series	R_1 (mΩ)	R_2 (mΩ)
2G	–	–
3B	2.2	0.7
4B	1.5	0.5
5B	1.5	0.3

Watertight series
Keyed watertight series



F series



Series	R_1 (mΩ)	R_2 (mΩ)
0E-0K	2.8	1.6
1E-1K	2.2	1.5
2E-2K	1.8	1.2
3E-3K	1.6	1.2
4E-4K	1.4	1.0
5E-5K	1.4	1.0
6E	1.0	0.5

Series	R_1 (mΩ)
0F	5.0
1F	3.0
2F	2.5
3F	2.5
4F	2.0
5F	1.5